Design of a Low-Power High-Speed T-Flip-Flop Using the Gate-Diffusion Input Technique

Soheil Ziabakhsh and Meysam Zoghi

***Abstract* —In this paper an implementation of a new TFF using GDI technique for low-power and high-speed in order to achieve a PDP is presently while having a still low complexity. Simulation results using ADS 2008 show that the proposed flip flop has the least propagation delay of 169.7 psec and consumption power 188.9 µW in a power supply of 1.8 V. Also results show more than 45% decrease in PDP of proposed circuit.**

***Keywords* — GDI, high-speed, low-power, PDP, T flip flop.**

I. Introduction

Wide utilization of memory storage systems and sequential logic in modern electronics triggers a demand for high-performance and low-area implementations of basic memory components.

In these circuits, the output not only depends upon the *current* values of the inputs, but also upon *preceding* input values. These circuits are often called cyclic logic circuits. These Timing elements (TEs) include latches, flip-flops, registers, and memory storage cells are one of the most important components in synchronous VLSI designs. Their performance has a critical effect on cycle time and they often account for a large fraction of total system power. Therefore, there has been significant interest in the development of fast and low power TE circuits, and correspondingly in techniques to evaluate their performance. Previous work in TE characterization [1-5] has failed to consider the effect of circuit loading on the relative ranking of TE structures. These earlier work used fixed, and usually overly large, output loads when comparing alternatives. Input drive was either assumed to be large [3, 5] or was not specified [1, 2, 4, 6, 7]. Bistable circuits exhibit two stable states representing logic one and logic zero. These include latches and flip flops, which are useful in a number of applications that require the temporary retention of one or more bits. Some examples are counters, shift registers, and memories. Bistable circuits can also perform signal shaping functions, e.g., the Schmitt trigger, which exhibits hysteresis and is useful in this regard. The two requirements for realization of bistable operation are amplification (gain greater than unity) and positive feedback. A circuit meeting these requirements can be built using two cross-coupled inverters, as shown in Fig. 1. There are two stable states for this circuit: state 0 is characterized by $Q = 0$ and $Q' = 1$ and state 1 is characterized by $Q = 1$ and $Q' = 0$ Either state is stable and will be maintained as long as the system power is on; therefore, this circuit can retain 1 bit of information.

T or toggle flip flop which is often used for counters can be realized by connecting the J and K inputs of JK flip flop together. All of the popular flip flop can easily be modified to incorporate asynchronous set and/or reset inputs. For master-slave inputs, this normally means adding some extra circuitry to both the master and the slave latch so that the asynchronous inputs will dominate independent of the clock and other inputs. These inputs are often used to initialize the state of digital ICs at the time the power is first applied. Normally, a set or reset input is required, but seldom both. A T flip flop alternately sends an output signal to two different outputs when an input signal is applied.

This paper proposes of a low-power high-speed T flip flop Using GDI Technique. This novel technique proposes a new method for designing logical circuits in standard technologies of CMOS and SoI.

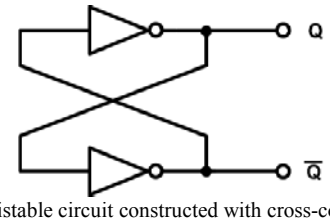

Figure 1: A bistable circuit constructed with cross-coupled inverters

II. Basic T Flip Flop

T flip flop with clock pulse is shown in Fig. 2. This particular configuration is the basis for many CMOS T flip flops, but it does suffer from a similar limitation as the SR flip flop. The characteristic table for toggle or T flip flop is described in Table I. This is equivalent with, if T is "0", the state will not change and if T is "1" then flip flop will change state or toggle.

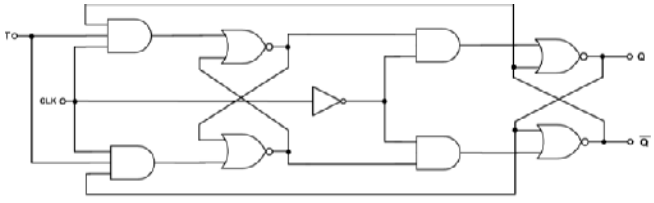

Figure 2: A T flip flop based on cross-coupled NOR gates.

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TABLE I: THE CHARACTERISTIC TABLE FOR A TOGGLE OR T FLIP FLOP.

	T	*Q*(*t*+1)
No Change	0	*Q(t)*
Toggle	1	*Q'(t)*

III. BASIC GDI FUNCTION

The GDI method is based on the simple cell shown in Fig. 3. A basic GDI cell contains four terminals - G (the common gate input of the nMOS and pMOS transistors), P (the outer diffusion node of the pMOS transistor), N (the outer diffusion node of the nMOS transistor) and the D node (the common diffusion of both transistors). P, N and D may be used as either input or output ports, depending on the circuit structure. Table II shows how various configuration changes of the inputs P, N and G in the basic GDI cell correspond to different Boolean functions at the output D. GDI enables simpler gates, lower transistor count, and lower power dissipation in many implementations, as compared with standard CMOS and Pass-transistor Logic (PTL) design techniques [8].

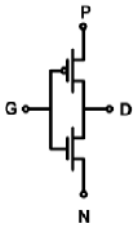


Figure 3: GDI basic cell

TABLE II: SOME LOGIC FUNCTIONS THAT CAN BE IMPLENTED WITH A SINGLE GDI CELL.

N	P	G	D	Function
'0'	B	A	$\bar{A}B$	**F1**
B	'1'	A	$\bar{A}$ + B	**F2**
'1'	B	A	A + B	**OR**
B	'0'	A	AB	**AND**
C	B	A	$\bar{A}B$+AC	**MUX**
'0'	'1'	A	$\bar{A}$	**NOT**

This paper presents a new implementation of low-power, high-speed TFF using GDI technique. This new design achieves lower PDP in compared with previous works. The circuits have been implemented in 0.18 µm TSMC CMOS technology and simulated to the proposed GDI structure with existing alternatives.

IV. DESIGN OF LOW-POWER, HIGH-SPEED GDI T FLIP FLOP

A novel implementation of a GDI TFF is shown in Fig. 4. It is based on the Master-Slave connection of two GDI Latches and some gates. Each latch consists of four basic GDI cells, resulting in a simple eight-transistor structure and gates consists six transistors in order that related with latch. The components of the latch circuit can be divided into two main categories; GDI gate and inverter. GDI gate uses two transistors and controlled by the Clk signal. Clk signals fed to the gate of transistors and create two alternative states: one state is when the Clk is low and the signals are propagating through PMOS transistors and create transient state and other one is when the Clk is high and the prior values are maintained due to conduction of the outputs. In this state, GDI gates holding state of the latch.

Other gates for main T flip flop are inverter gates. They are responsible for maintaining the complementary values of the internal signals and the circuit outputs. Note that the size of the p-channel transistor is wider than that of the n-channel transistor. This width difference is not needed for functionally correct operation. Rather, it somewhat compensates for the difference in the motilities of n-channel and p-channel transistors. The effective mobility of n-channel transistors is between two and four times that of p-channel transistors. These inverters has important role for swing restoration and improved driving abilities of the outputs, it's buffering of the internal signals and create suitable output current for driving of load.

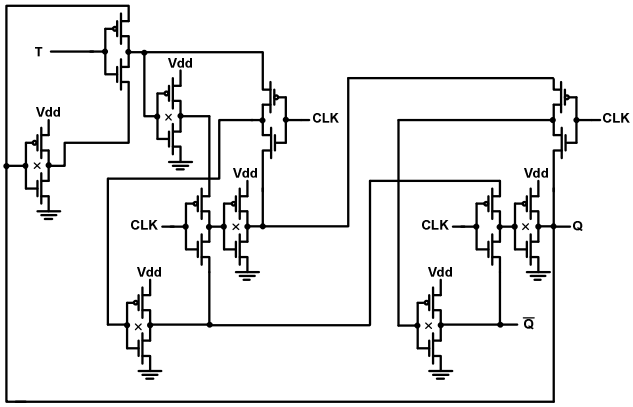


Figure 4: GDI T flip flop implementation.

V. SIMULATION RESULTS

A T flip flop designed in GDI and two kinds of CMOS was simulated in 0.18µm TSMC CMOS [9] technology. Simulation results shows compare the GDI design with a set of representative flip flops, commonly used for high performance design. The circuits were simulated using ADS 2008 at 1.8V, 500 MHz and 27 ^{0}c, with load capacitance of 100fF. The simulation setup is shown in Fig. 5. The device under test was placed between input buffers to account for the current consumption from the previous stage, and output buffers to emulate real environmental conditions.

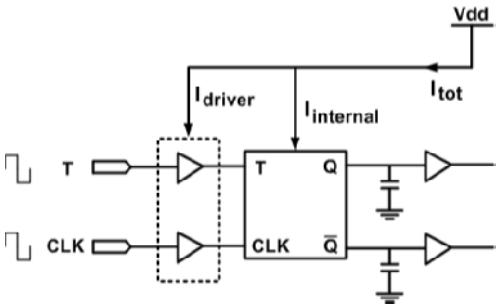


Figure 5: Simulation setup.

The reference circuits are presented in Fig. 6. The set includes (a) modified CMOS after and (b) TGB after [10]. These circuits have been sized according to optimization procedure, as presented in [10].

Fig. 8 shows timing diagram of input clock, square input wave, output of T flip flop (Q) and its differential output (Q') for proposed T flip flop. The comparative results are presented in Table III. The best results in each compared category are emphasized. It can be seen, that GDI TFF outperforms the other circuits in terms of power-delay product and total gates area in both technologies (including the inverted inputs).

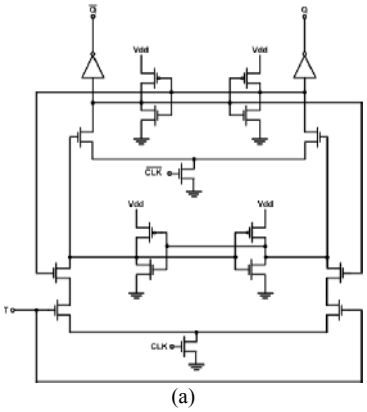
1) Average Power*:* Best results of average power are observed for the dynamic GDI ~ 77 % (approximately) less than the modified CMOS implementation and 84% less than the TGB circuit (which is the best CMOS implementation in terms of power). GDI T flip flop show results close to the CMOS circuit, and better than any static CMOS implementation.

2) Maximal Delay*:* The Dynamic GDI is the fastest circuit, showing up to 44% decrease compared to modified CMOS techniques, and a 76% improvement compared to the TGB, which is the fastest technique among CMOS circuits.

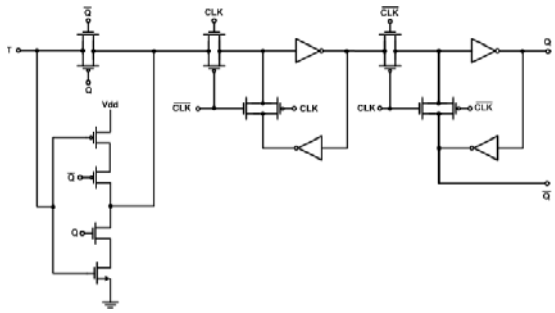
3) Power delay product*:* GDI T flip flop circuit has 87% decrease PDP compared to modified CMOS technique and 96% less than TGB circuit.

It should be noted that the optimization in all compared circuits is performance-driven (minimal power-delay product is obtained by sizing), while separate parameters, like average power and maximal delay are secondary. The Simulation results diagram obtained through can be seen in Fig. 8 for Average power and PDP used.

The layout of the proposed low-power, high-speed TFF is presented in Fig. 9.

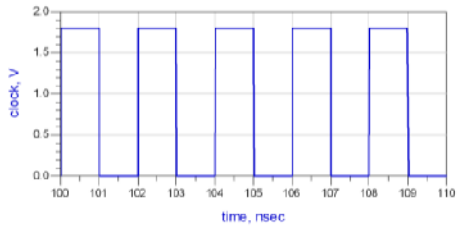


(a)

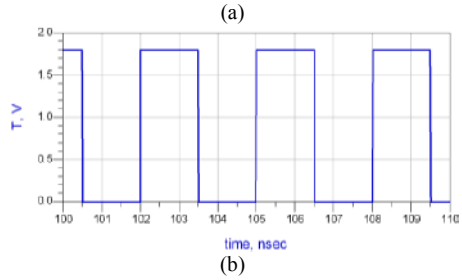


(b)

Figure 6: Set of representative flip-flops for comparison: (a) modified CMOS, (b) TGB



(a)



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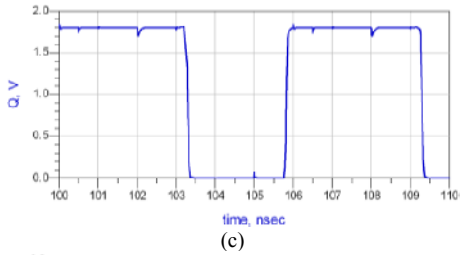

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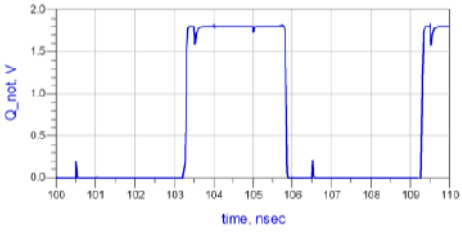
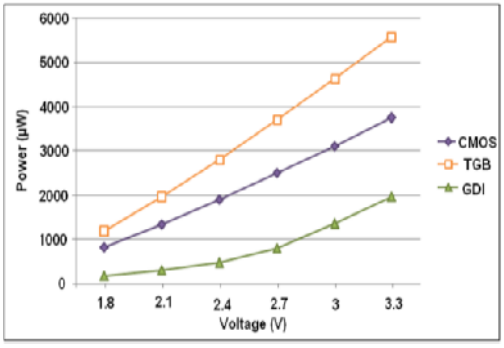
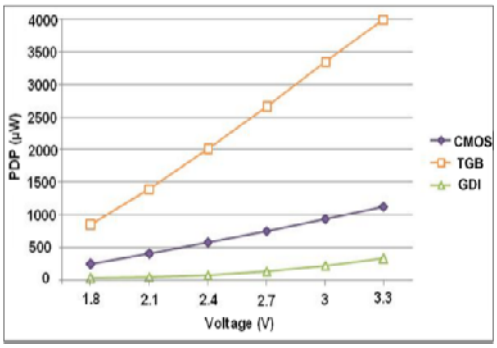


(d)

Figure 7: timing diagram of a) input clock, b) square input wave, c) output of T flip flop (Q) and d) differential output (Q')



(a)



(b)

Figure 8: Simulation results diagram and comparison of modified CMOS, TGB and GDI for a)Average power and b) PDP used.

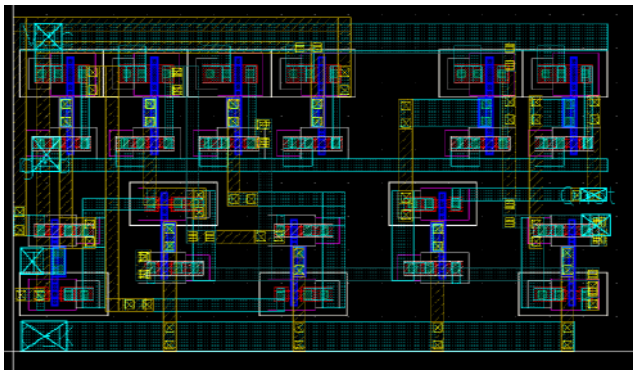


Figure 9: Proposed CMOS T flip flop layout.

VI. Conclusion

A novel methodology for asynchronous circuits, based on two-transistor GDI cells, was presented. In this paper we proposed a GDI T flip flop for low-power design was presented. The proposed circuit has a simple structure, based on two Master-Slave principles, and some gates to describe T flip flop. It contains 24 transistors. An optimization procedure was developed for GDI TFF, based on iterative transistor sizing, while targeting a minimal power-delay product. Performance comparison with other TFF design techniques was shown, with respect to gate area, delay and power dissipation.

Simulation results in 0.18 µm CMOS process show that the proposed T flip flop has the least propagation delay of 169.7 psec, consumption power 188.9 µW and power delay product 32.05fJ in a power supply of 1.8 V.

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TABLE III: SIMULATION RESULTS FOR 0.18µm TSMC CMOS TECHNOLOGY.

Circuit	Number of Transistors	Total Width [µm]	CLK- Q (LH) [ps]	CLK- Q' (HL) [ps]	CLK- Q (HL) [ps]	CLK- Q' (LH) [ps]	Power [µm]	Max Delay [ps]	Total PDP [fJ]
Modified CMOS	24	36.9	301.2	134	122.9	145.4	827.48	301.2	249.23
TGB	26	41.76	715	126.5	124.1	132.8	1189.15	715	850.24
GDI	**24**	**6.82**	**131.6**	**167.5**	**169.7**	**168.5**	**188.88**	**169.7**	**32.05**