A Low Noise Figure, High Conversion Gain CMOS LNA for 2.4 GHz Application

Soheil Ziabakhsh and Alireza Saberkari

***Abstract* — This paper presents a CMOS LNA with modified input matching network and based on the current reuse approach that leads to better performance in terms of NF, and CG for low supply voltage applications. In the proposed architecture, two combinations of the SID and SL methods are used to convert the input to 50 Ω.**

***Keywords* — LNA, Input Matching, Noise Figure, Power Dissipation, Conversion Gain.**

I. Introduction

RECENTLY, demand for a low-cost low-power wireless transceiver utilizing standard CMOS technology has been increased, significantly [1]. Especially with the introduction of the IEEE 802.15.4 ZigBee standard, which is a low-rate, low-cost, and low-power network [2], these demands tend to dominate transceiver developments. The standard has numerous markets and applications for this low data-rate standard such as industrial and commercial, home automation, consumer electronics, personal health care, games, etc. that should be able to operate for six months or two years on just button cells or battery [3].

The most severe consequences of the technology scaling, that affects RF analog designers, is a reduction of the supply voltage. Insufficient voltage room causes that some circuit topologies cannot satisfy the required specifications or even they cannot operate. Hence, research on low voltage circuit topologies is important. The most challenging building block in the front-end receiver is the low noise amplifier (LNA) which precedes a high noise figure stages such as image reject filters, mixer, etc [4]. The basic function of the LNA is to provide signal amplification while adding as little noise and distortion as possible to improve the overall noise figure and linearity of the front-end. This work presents the design and simulation of a 1.5 V CMOS LNA with modified input matching network that leads to a better performance in terms of noise figure, power consumption, and conversion gain for low supply voltage applications. The proposed LNA is designed to be integrated in a direct conversion receiver with successive stages being balanced to minimize second order effects such as DC offsets.

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II. Input Matching Architectuers

Two different input matching techniques used in the design of narrow band CMOS LNAs are discussed in this section. These techniques are used to match the input of LNA to the output of antenna, which usually equals to 50 Ω, preceding it to minimize reflections between the LNA and antenna.

A. SID

Source inductive degeneration (SID) is one of the most popular input matching methods in the design of LNAs [5], [6]. As shown in Fig. 1(a), SID employs a small inductor L_s in series with the source of the MOSFET to generate a real 50 Ω resistance at the input of the LNA. The imaginary part of MOSFET's input impedance is cancelled by another inductor L_g located at the input of the LNA. It is well known that the value of the real resistance generated by L_s is approximately given by $R_s = g_m L_s/C_{gg} = \omega_T L_s$ where $C_{gg} = C_{gs} + C_{gd}$ and $\omega_T = 2\pi f_T$ is the unity current gain frequency of MOSFET transistor. Using the small signal equivalent circuit of the LNA shown in Fig. 2(a), the input impedance seen at the input of the LNA, $Z_{in\text{-}SID}$ is given by

$$Z_{in-SID} = 1/\left(j\omega C_{gg}\right) + R_p + \omega_T L_s + j\omega\left(L_g + L_s\right) \quad (1)$$

where R_p is the parasitic input resistance of the MOSFET. To match the input of the LNA, $(R_p+\omega_T L_s)$ and $(L_g + L_s)$ should be equal to 50 Ω and $1/(\omega^2 C_{gg})$, respectively. Although this technique is suitable to match the input of the LNA to 50 Ω, it degrades the power gain of the LNA. Therefore, the dc power consumption of the LNA has to be increased to meet the power gain requirements of the system, which will in turn lower the battery life time of mobile systems and hence, may not be suitable for low-power applications.

B. SL Method

Series L (SL) method, shown in Fig. 1(b), is another way for input matching which uses a simple LC network at the input of LNA [7], [8]. According to the simplified small signal equivalent circuit of the LNA shown in Fig. 2(b), the input impedance, $Z_{in\text{-}SL}$ of the LNA is given by

$$Z_{in-SL} = \frac{R_p + j\omega\left[L\left(1-\omega^2 LC_p\right) - C_p R_p^2\right]}{\left(\omega C_p R_p\right)^2 + \left(1-\omega^2 LC_p\right)^2} \quad (2)$$

where R_p is the parasitic input resistance of the MOSFET, $L = L_g - 1/(\omega^2 C_{gg})$, and $C_{gg} = C_{gs} + C_{gd}$. To match the input of the LNA, the imaginary part of $Z_{in\text{-}SL}$ should be equal to zero and its real part to 50 Ω and hence,

$$L = \frac{\sqrt{50R_p - R_p^2}}{\omega} \tag{3}$$

and

$$C_p = \frac{\sqrt{50R_p - R_p^2}}{(50\omega R_p)} \tag{4}$$

Equations (3) and (4) show that the parasitic input resistance of MOSFET can be easily converted to 50 Ω by properly choosing the values of L_g and C_P, hence, eliminating the need for L_s. In addition, the frequency at which the return loss S11 reaches its minimum and the value of minimum return loss can be adjusted by L_g and C_P, respectively.

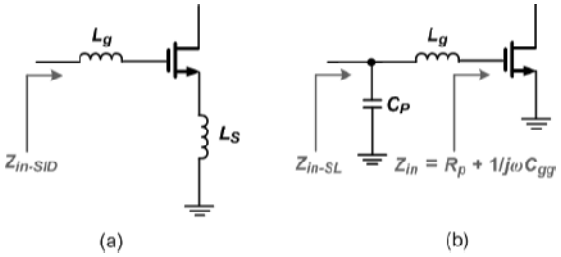


Figure 1: (a) SID, (b) SL matching methods.

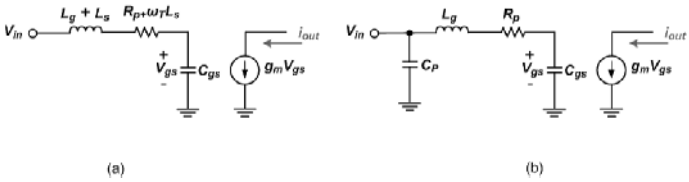


Figure 2: Simplified equivalent circuit model of the input stage of LNA used (a) SID and (b) SL methods.

It is demonstrated that the SL method does not necessarily degrade the noise figure of the LNA if the transistor sizes and passive elements are chosen carefully [8].

III. Proposed LNA With Modified Input Matching

A. Design of the RF Input Narrow-band Network for the LNA

The input matching network of the LNA is designed using two combinations of the SID and SL methods for 2.4 GHz application to achieve the best noise figure and input matching. It is known that in a CMOS LNA there are several noise sources: channel noise, gate induced noise [9], thermal noise of various parasitic resistances, etc. Fig. 3 illustrates a simplified small signal model for RF input LNA noise figure (NF) calculation. Based on Fig. 3 and according to the MOSFET noise analysis in [9] and [10], the noise factor (F) of input of LNA is derived as:

$$F = 1 + \frac{R_\Delta}{R_s} + P_2\ P_4 \frac{3}{2P_5 L_{eff} C_{ox}} \frac{1}{\sqrt{I_{ds} W}} + \left[P_2 P_3 P_4 + P_1 P_2\right] \omega_0^{\,2} \frac{2L_{eff} C_{ox}}{3P_5} \frac{W^{\frac{3}{2}}}{\sqrt{I_{ds}}} \tag{5}$$

where ω_0 is the resonant frequency and R_Δ is sum of the parasitic resistances which generates thermal noise and including sum of the gate resistance of the NMOS device (R_g) and the series resistance of the inductor L_g (R_l) [11]. W and L_{eff} are the total gate width and length of the input transistor and I_{ds} is the current through it. Coefficients P_1-P_5 are as follows;

$$P_1 = (R_s + R_1)^2 + 2(R_s + R_1)^2 |c| \sqrt{\frac{\delta\alpha^2}{5\gamma}}$$

$$P_2 = \frac{\gamma}{R_s \alpha},\quad P_3 = (R_s + R_1)^2,\quad P_4 = \frac{\delta\alpha^2}{5\gamma} \tag{6}$$

$$P_5 = \frac{\left[\frac{2}{\xi L_{eff}} \mu_{eff} C_{ox}\right]^{\frac{1}{2}}}{\frac{2}{3} L_{eff} C_{ox}}$$

Parameters such as δ, α γ, c, and ξ can be found in [11].

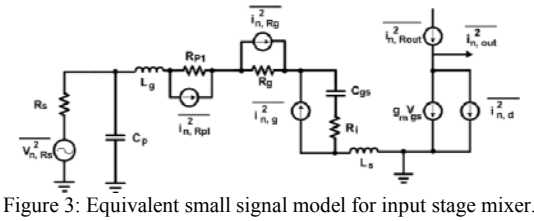


Figure 3: Equivalent small signal model for input stage mixer.

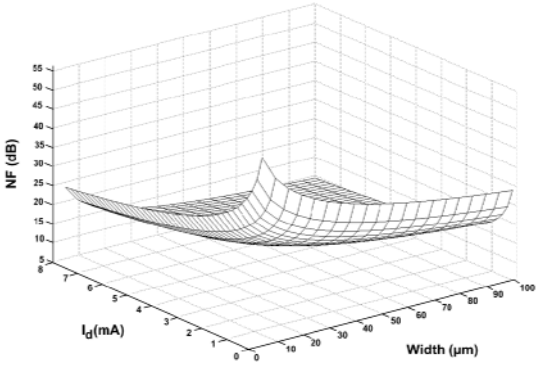


Figure 4: noise figure (NF) verses I_d and W.

Figure 4 illustrates the relation between NF, I_d, and W in terms of (19). The plot shows the LNA has an optimum W around 80 μm, which corresponds to NF_{min} when I_d is fixed. Generally, noise optimization is a process to find the optimum device size, so that a relative low NF can be obtained, while giving consideration to the input reflection coefficient, power consumption, etc. In this work, I_d = 6 mA, W = 80 μm are finally chosen. Although the NF is high comparing with its counterpart using high-Q off-chip inductors, it is compact and fully integrated. After selecting the device size, based on the simulation results, for having improvement in the overall performance of the LNA, the parallel capacitance (C_P) is added to achieve the best input matching.

B. Design of the 2.4 GHz LNA

Schematic diagram of the LNA is shown in Fig. 5. In this circuit, both pairs of $M_{1,2}$ and $M_{5,6}$ operate as common-source stages and share the same bias current. The signal amplified by $M_{1,2}$ is coupled to the gates of $M_{5,6}$ by C_1 while the source of $M_{5,6}$ is bypassed by C_2. The circuit thus saves power through the reuse of the bias current. In practice, the parasitic bottom-plate capacitance of C_1 may limit the RF gain at gate of $M_{5,6}$ and drain of $M_{3,4}$. The cascode structure is used in the design of this circuit to provide higher isolation and gain. Another advantage of

using the cascode device is that, it basically shields the output from the input stage and highly increases the reverse isolation, S12. The size of the cascode transistor is chosen based on the required value of R_{in} as g_m of this transistor directly affects the input resistance of the LNA. Therefore, the width of the cascode device is chosen 30 µm which is lower than half of that of the common-source transistors. Subsequently, the simulated Z_{in} of the cascade structure at f = 2.4 GHz becomes Z_{in} = 37.35 – j 793.7. Using this Z_{in} in (3) and (4), the initial values for L_g and C_P are obtained as 27.7 nH and 770 fF, respectively. However, due to the trade-off between NF and S11 in the SL method, simulations are carried out to optimize the values of L_g and C_P, which finally results in L_g = 28.41 nH, and C_P = 770 fF. However, since the required R_{in} is larger than $R_{in\text{-}SL}$, an inductance around 100 pH is added to the source of $M_{1,2}$ for better impedance matching. The use of inductive source degeneration through L_s has the benefit of simultaneous input matching and noise improvement.

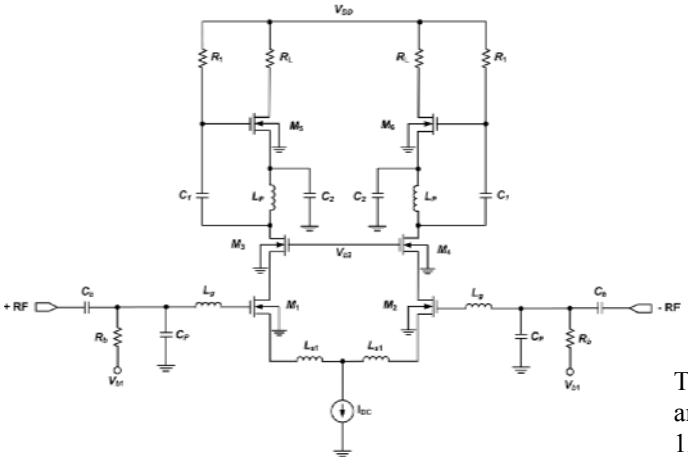
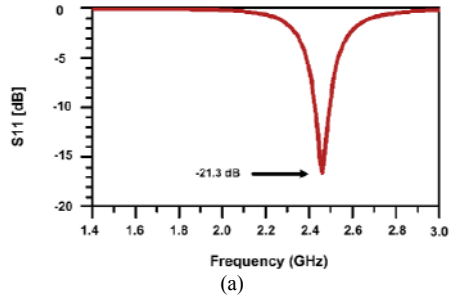


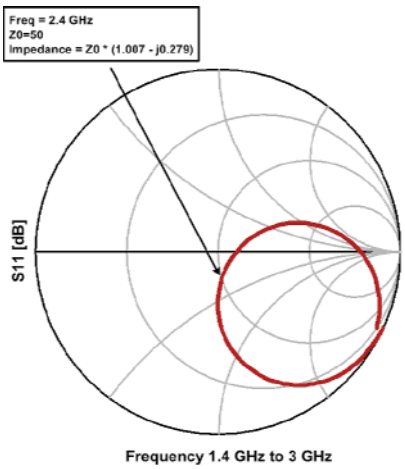
Figure 5: Schematic diagram of a 2.4 GHz proposed LNA based on the SID and SL input matching.

IV. Simulation Results

The proposed LNA is simulated in TSMC 0.18 µm CMOS process by ADS. Figure 8 shows the input return loss S11 and Smith chart of the LNA. The plot shows that S11 is lower than -20 dB at 2.4 GHz and Smith chart shows the best input matching (Z_{in}) of LNA.



(a)



(b)

Figure 6: Input matching characteristics a) S11, b) Loci Z_{in} in the Smith chart.

The noise figure performance of the LNA is shown in Fig. 7. As can be seen, the noise figure is 1.81 dB at 2.4 GHz.

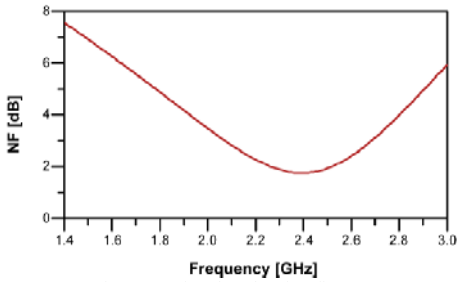
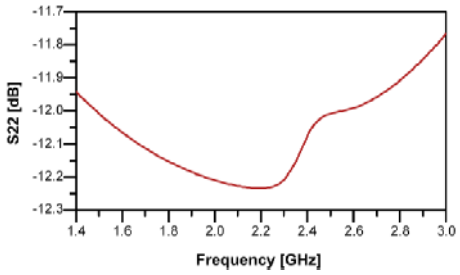
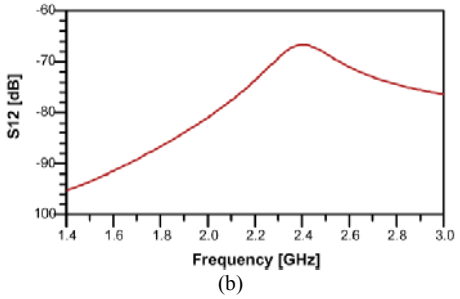


Figure 7: simulated noise figure.

The plots shown in Fig. 8 are the output return loss S22 and S12 at 2.4 GHz frequency. As can be seen, the S22 is -12.08 dB and S12 is -66.68 dB at 2.4 GHz.



(a)



(b)

Figure 8: simulated a) S22, b) S12.

As shown in Fig. 9, it is found that the LNA performs a small signal gain (S21) of 18.01 dB with a 3-dB gain bandwidth of 250 MHz.

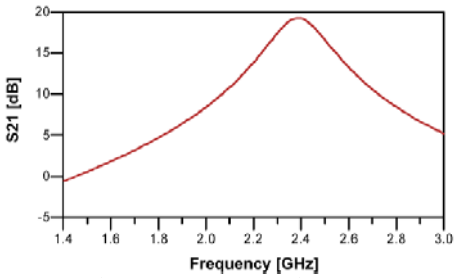


Figure 9: LNA power gain (S21).

Performance of the proposed LNA in comparison with other LNAs is summarized in Table I. As can be seen, the proposed LNA has reached to a sufficient conversion gain and input matching in parallel with an excellent noise figure. Table I clearly shows that the proposed LNA's performance is better than previous works however its power consumption in comparison with others is suitable.

V. Conclusion

This paper has presented a CMOS low noise amplifier (LNA) based on the current reuse approach and with modified input matching network which is in combination of two SID and SL methods to convert the input of MOSFETs to 50 Ω. The effect of the used matching network on the power gain and noise figure of the LNA is shown that by this method a very low noise LNA can be achieved while its power consumption is relatively low. The results indicate that the proposed LNA has achieved to a conversion gain of 18.01 dB, noise figure of 1.81 dB, and input matching (S11) of -21.3 dB at 1.5 V supply voltage while its power dissipation is 9 mW. Moreover, it is demonstrated that the *NF* and power dissipation of the LNA can be minimized by properly choosing the size of the active and passive components. The proposed LNA also achieves the best overall performance in comparison with the most recently published works.

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TABLE I
SUMMARY PERFORMANCE OF THE PRESENTED LNA AND RECENTLY PUBLISHED RESULTS.

Reference	CMOS Process	Matching Method	Frequency [GHz]	S11 [dB]	Gain [dB]	NF [dB]	P_{diss} [mW]
[12]	0.18 µm	PLC	5.7	<-10	14.2	2	21.6
[13]	0.25 µm	PLC	1.7	<-10	12	1.8-3.4	40
[14]	0.18 µm	PLC	2.4	-10.1	10.1	2.9	11.7
[15]	0.18 µm	PLC	2.4	-16	24	2.7	15
[16]	0.35 µm	SID	2.4	<-33	6	4.8	-
[17]	0.35 µm	SID	2.2	<-13	8.6	1.92	8.1
[18]	0.13µm	SID	2.1	-14	5.2	3.0	12.6
This work	**0.18 µm**	**SID + SL**	**2.4**	**-21.3**	**18.01**	**1.81**	**9**