

Software Controlled Digital FM Modulator for 100 Standard Stations

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Abstract — The purpose of this paper is to present the design of the system for multichannel radio signal distribution in the standard FM broadcast band. Realization techniques are closely coupled with the latest digital signal processing algorithms and specially adapted for new market-available electronic devices. Comparing with the similar of-the-shelf, one-channel systems, the price of the product and its power consumption are significantly lower.

Keywords — DSP, FM modulator, FPGA, multirate system, satellite radio.

I. INTRODUCTION

IMPOSING the *digital signal processing* (DSP) theory into the new market available electronic components it is possible to produce custom-designed systems on a *field programmable gate array* (FPGA) chip. Such a design can replace existing and complex dedicated systems in all aspects and adapt widely disseminated infrastructures to the new technology. This approach is used in the design of implemented *Digital FM Modulator* for 100 standard stations [1]. Its usage is mainly in applications for the local distribution of a satellite radio signal. The device should replace existing similar systems and make available the reception of a satellite radio program to standard FM radio receivers, in urban environments [4].

The price of a similar of-the-shelf product is about from \$ 100 to \$ 1000, and it is only for a one-channel transmission. For a particular number of audio streams, it is necessary to by many boxes to form desirable system configuration. With this FM modulator, the cost, package dimensions and power consumption will be significantly reduced, retaining the same CD-quality broadcasting.

Another advantages lie in the parallel processing of the all channels and a modular approach in the system design that enables easy testing and flexible capabilities upgrade.

This paper will describe the employed design techniques, integration for the entire system divided into the units (audio signal processing, FM and frequency-division multiplex), USB interfacing and the software control and the hardware test platform and development tools.

II. DESIGN TECHNIQUES

In order to achieve such a specific system demands (high frequency and fast development cycle), the following design and optimization techniques have been used:

- *Time-division multiplexing (TDM)* – According to the high system clock frequency (192 MHz), there is an ability to process all of the 100 audio signals (at the sampling rate lower than 400 KHz) by a single module (maximum 4 clock cycles per channel).
- *Pipelining* – Each of the larger combinatorial logics (multiplexer, adder, multiplier, ...) must be pipelined to reach the high system clock frequency.
- *Reusing Resources* – Processing the largest possible number of signals by a single module to increase the hardware usage.
- *Designing multirate filters* – DSP technique for processing of signals with different sampling rates [11].
- *Interpolation* – signal resampling [8] [11], linearization between samples.
- *Frequency-division multiplexing (FDM)* – Each of the TDM signals is assigned to a non-overlapping frequency band (200 KHz wide) in the defined range (88 – 108 MHz).
- Simultaneously processing of two samples to reach the sampling frequency (384 MHz), which is higher than the system clock frequency (192 MHz).

III. AUDIO SIGNAL PROCESSING

The input signal sampling rate is 48 KHz. The format is defined as fixed point 16-bit data in the time-division multiplex, with synchronization signal. The first group of the designed blocks (Fig. 1 and Fig. 3) is used to create the time-division multiplex of the 100 stereo composite signals and prepare them for the FM modulation.

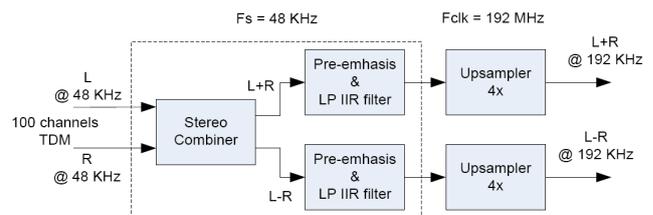


Fig. 1. Creating the $L+R$ and $L-R$ components in audio processing block.

A. Stereo Combiner

The arithmetic signal encoding from the stereo component signals *left* and *right* (L and R), to the $L+R$ and $L-R$ stereo components is done with the *stereo combiner*. The module encloses an adder and a subtractor, which produce the output signals in *fix_18_17* format (18 bits wide word and 17 bits wide binary fraction). This format is used, because the hardware multiplier has two 18-bit operands, and the result of the multiplication should be in the range from -1 to 1.

B. Pre-emphasis & LP IIR Filter

This filter is realized as an *infinite impulse response* (IIR) filter [8] (Fig. 2), because of its low sampling rate and a quite narrow transition band (15 – 19 KH at the 48 KH sampling rate). It is used to increase the amplitude of the signal frequency components (higher than 3.183 KHz), to improve the signal-to-noise ratio. A single-zero analog filter is transformed to a digital filter, using the *bilinear transformation method* [8] [9].

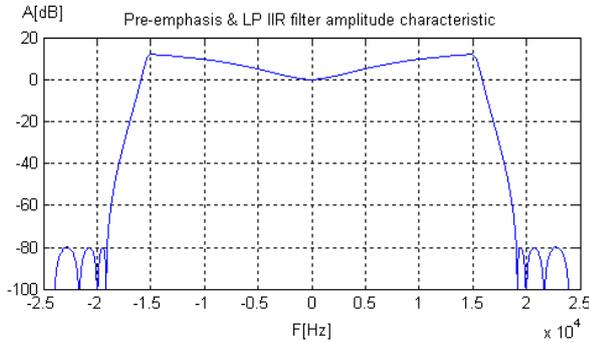


Fig. 2. Impulse response amplitude spectrum of the pre-emphasis and LP filters conjunction.

The IIR filter is composed of four *second order sections* [1] which include coefficients of the filters conjunction. Each of the sections operates with floating point numbers and calculates the result of the *multiply and accumulate* (MACC) operation in the same format [3]. Before the IIR filter, the input signal is converted into the floating point format, and after the filter, back to the fixed point format. This format is used due to the fact that the calculation result between the sections pretends to overflow the maximum amplitude range.

C. Fixed Upsampler 4x

In this system, the audio signals have to pass the several upsampling levels. First of them is the upsampling from 48 KHz to 192 KHz (Fig. 1). Three samples are interpolated and inserted between every two samples of the input signal. Upsampling is done in order to accomplish the next operations: up-conversion of the $L-R$, and its addition to the $L+R$ component (Fig. 3).

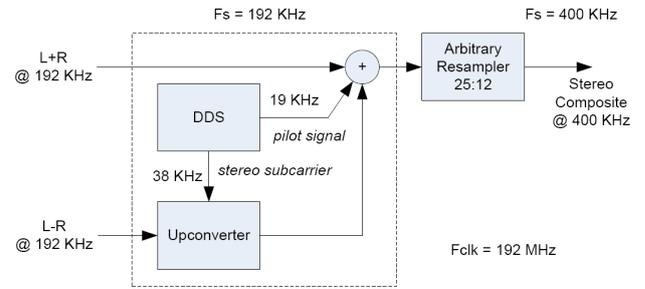


Fig. 3. Preparing the 100 stereo composite signals in TDM, for the FM modulation.

D. Creating the TDM Stereo Composite Signal

Multiplying the $L-R$ with the referent sinusoidal signal (*stereo subcarrier* in Fig. 3), the component is shifted in the frequency domain at the 38 KHz central frequency. The *pilot signal* (19 KHz sinusoidal signal) is in a relation with the stereo subcarrier and it is used by the stereo decoder at the reception-side, to get back the separated L and R components.

E. Arbitrary Resampler

The sampling frequency 48 KHz is a product of the oscillator on the motherboard of the system, which sends the input audio streams. Synchronization between those systems is accomplished by designing an *arbitrary resampler*, whose ratio is variable around the value 25:12. An arbitrary resampler performs interpolation of a sampled data signal, computing sample values of an underlying analog signal located on one set of periodically spaced sample locations from data samples located on another set of periodically spaced sample locations [10].

To avoid the FIFO buffer overflow with input audio samples, the arbitrary resampler is self-controlled by a proportional-integral regulator, expressed by the equation:

$$s = s_0 + \hat{s} = s_0 + K_p e(t) + K_i \int_{-\infty}^t e(\tau) d\tau, \quad (1)$$

where the relevant parameters are:

- s – accumulation step,
- s_0 – constant step value,
- \hat{s} – step correction,
- K_p – Proportional gain; a tuning parameter,
- K_i – Integral gain; a tuning parameter and
- $e(t)$ – error signal; variation of the number of samples in the buffer around the *half full* value.

The sampling rate of the output signal is 400 KHz. In its control block, the most significant counter, in the triple control hardware “for” loop, is replaced by a 32-bit accumulator, whose integer part is used for filter bank addressing, and the fraction for the linearization between adjacent banks.

The *linearization* process is described by the equation (2) and Fig. 4.

$$C = XB + (1 - X)A. \quad (2)$$

The meanings of the parameters are:

- C – approximated value,
- A and B – output samples calculated for two adjacent FIR filter banks in the circular process and
- X – fraction of the accumulated value in the range from 0 to 1 (accumulator in the control block).

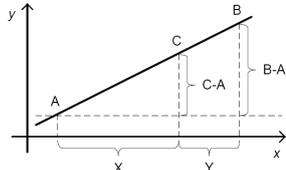


Fig. 4. Linearization.

Amplitude spectrum of the stereo composite signal which is to be FM modulated is shown in Fig. 5.

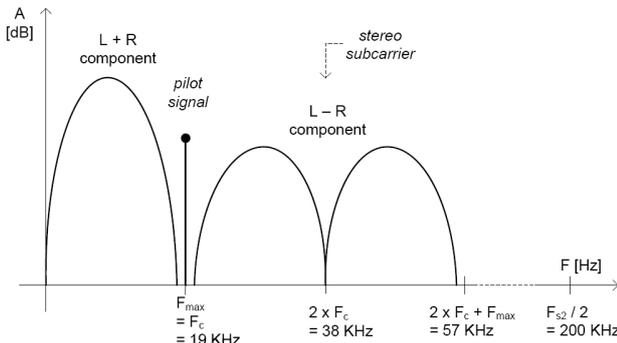


Fig. 5. Amplitude spectrum of the stereo composite signal at 400 KHz sampling rate.

IV. FM AND FREQUENCY-DIVISION MULTIPLEX

The second group of the designed blocks (Fig. 6 and Fig. 9) is used to create the 100 FM modulated stereo composite signals, and to multiplex them in a single frequency-division multiplex at the 384 MHz sampling rate.

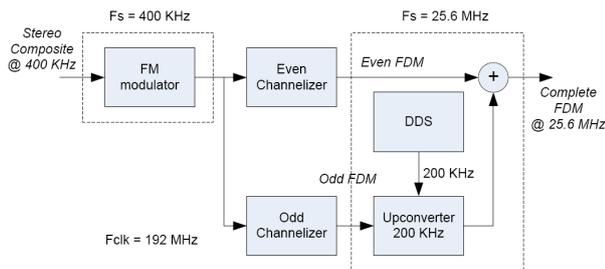


Fig. 6. Creating an FDM of the 100 FM stereo composite signals.

A. FM Modulator

FM modulator is accomplished as a numerically controlled oscillator (NCO) [1], which generates a sinus and a cosines signal. NCO accumulation step is able to be changed by input signal (in this case, the input is TDM of 100 stereo composite signals).

The Fig. 7 shows an output signal of the FM modulator, when the input signal is sinusoidal and its frequency is 5 KHz. The output signal is composed of the sinusoidal components at the integer multiples of the input signal frequency.

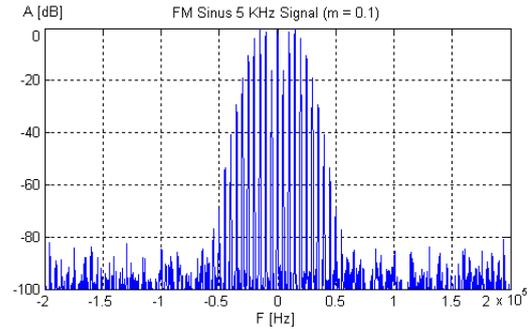


Fig. 7. Result of the FM modulated sinusoidal input signal (frequency: 5 KHz and modulation index: 0.1).

B. Channelizer

This module is used to convert the TDM into the FDM. There are two *inverse fast Fourier transformation* (IFFT) modules [12] inside the *channelizer* [11], which arrange the TDM signals (50 even and 50 odd channels separately) by particular bands, and convert them into the two single FDM signals.

The Fig. 8 shows an FDM signal of the 100 channels in natural order (0, 1, ..., 99 – from left to right), in range -20 – 20 MHz. Each of the bands is 200 KHz wide.

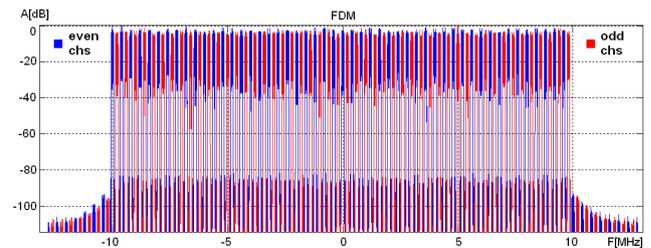


Fig. 8. Amplitude spectrum of the complete FDM signal.

C. Upconverter 200 KHz

The odd FDM signal is shifted at the 200 KHz central frequency by this module, and it is prepared for the addition to the even FDM. In the base of the upconverter is a complex multiplier, which operates with the complex input signal (odd FDM) and the complex sinusoidal signal, generated by the *direct digital synthesis* (DDS) block (Fig. 6) [1].

D. Resampler 15:2 and Upsampler 2x

These two blocks (Fig. 9) are used for the FDM signal upsampling. The final product is a FDM signal at the 384 MHz sampling frequency, prepared for final upconversion to 98 MHz central frequency.

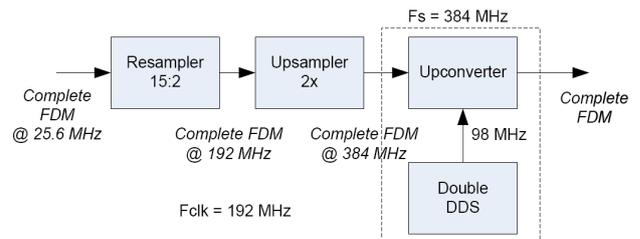


Fig. 9. Final resampling and upconversion to the frequency 98 MHz.

Upsampler 2x is able to process two samples per clock cycle, and to produce the output signal with the sampling frequency higher than system clock frequency.

E. Upconverter 98 MHz

Double DDS (in Fig. 9) is similar to the DDS module, but is capable to generate an even and an odd sample, simultaneously. By this module, the complex input signal is shifted in frequency domain at the central frequency of the standard FM broadcast band: 98 MHz for the range from 88 to 108 MHz [5].

V. SOFTWARE CONTROL

Software control allows a user to set some of the parameters in the design, and is realized by designing a *graphical user interface – GUI* (Fig. 10) which communicates with the design on the chip via the *USB debugging interface*. There is an API composed of several MATLAB functions, which exists as a support for the USB debugging interface.

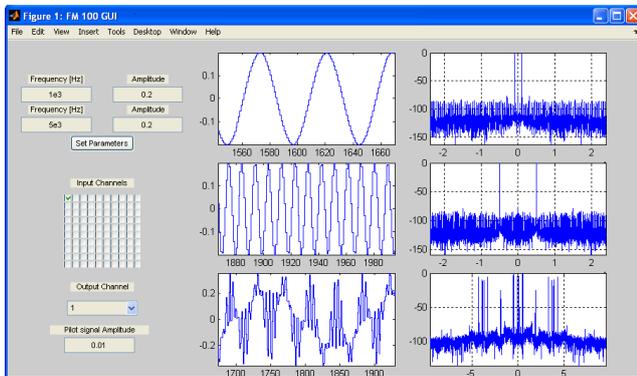


Fig. 10. A screenshot of the FM 100 GUI during a test.

VI. TEST AND RESULTS

The design has passed a complete synthesis and implementation process, from the model to the final hardware device. It has been tested on the board using the complete hardware and software platform composed of the following items:

- Development board with *Virtex 4 SX55-FF1148* FPGA chip [6],
- *MATLAB 2007a* with *Simulink* toolbox [16],
- *System Generator for DSP* [7],
- *Synplicity Synplify Pro 9.0.1* [17],
- *Xilinx ISE 9.2* [15],
- *Xilinx Platform Cable USB* [15] and
- *USB debugging interface* with *Spartan-3* FPGA chip.

A test session for the audio processing part is presented in the Fig. 10. There are *L* and *R* sinusoidal signals generated by an on-chip DDS module, and the composite stereo signal at the output of the audio processing block.

VII. CONCLUSION

The importance of the work is reflected in supporting the development of new technologies and their adaptation to existing infrastructures. From the economic point of view, the final product is more efficient, flexible; it can be widely available and less expensive than existing similar products.

The design could be upgraded by implementing an *RDS* support [14]. Using the *MATLAB Builder for Java*, the software could be compiled into a Java class, to be runnable by a Java virtual machine, and therefore – become portable.

For further design upgrades, it is advisable to take advantages of the *partial reconfiguration* [13], because of the long synthesis and implementation process. Compiling process of the complete design requires a long time. It is much faster to develop the design module-by-module, and incorporate it onto the chip, while the other successfully tested modules are still operating.

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