Using the Hilbert Transform in Modem Designing based on DSP processor for PLC

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***Abstract* — One of the most important parts of the data transmission systems is processing of the signals. In the primary models of this system, all these processes were done in an analog format. Because of this, the volume and the price were high. But in this model of system, however, all the processes are done digitally in which case the precision is high and also it contains all the abilities of the digitized systems. Some of the major changes in the structure of the system are: low cost, high precision, flexibility, etc.**

The main purpose of this Paper is analyzing base band processes, Modem by the Fixed-Point DSP processor. In this respect, the importance of the processor, its place and its operation is described will be made on the TMS320 DSP processors made by Texas Instruments (TI) company. Following this will be the analysis of the base band digital processor block diagram and the block diagrams of the digital process of the transmit (VF, HF) path. The block diagrams of receive (VF, HF) digital process is then described and also the block diagram of the SSB demodulator by the Fixed-Point DSP processor. Lastly there will be the conclusion of this Paper.

***Keywords* — Modem, Power Line Carrier, DSP Processor, Hilbert Transform.**

I. Introduction

The data transmission system has been designed fully digitized where the HF modulation and demodulation and the VF process is done by the Fixed-Point DSP processor. Also the entire also voice and telegraphy band filters in transmit and receive paths are fully digitized. figure (1) shows an overview of this data processor in the data transmission system.

II. The TMS320 family of processors overview

The importance of DSP processors is in the strong capability to calculate and process signals. We implemented two modems with two different TMS DSP's for studying the capability of DSP's and modems. Therefore we used identical algorithms for two platforms. The speed of TMS320C50 is 40 MIPS[1] and the speed of TMS320C5402 is 100MIPS; this means that each one-cycle command can be done in 25ns. Some of the abilities of this DSP are: flexible commands, process flexibility, high speed processing, innovated design of parallel structures and low cost.

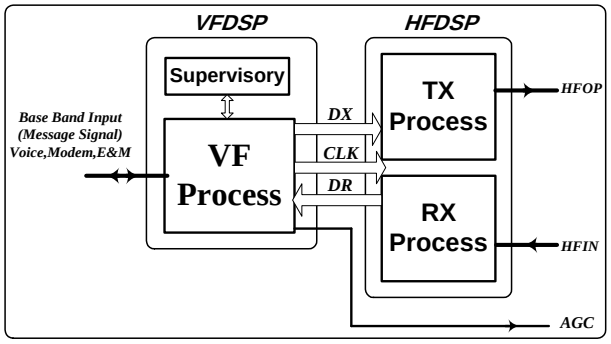

Fig. 1. Digital data processor block diagram in the data transmission system

III. Implementation the SSB modulator with using of DSP

The overall block diagram of the SSB modulator in the Fixed-Point DSP processor is as shown in figure (2).

FIR filter

The applicable digital filters are divided into Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) groups in communication systems. But for the two following reasons the FIR filters are used in DSP. First is that these filters are very important because of their linear phase, and second is that they are easy to come off by DSP and as we will see later on, only by the MACD instruction they can be made. We can easily claim that this filtering is in the nature of the DSP.

Assume that the goal is to create a FIR filter with N Taps and the coefficient of $C_{N-1}, \ldots, C_1, C_0$. Now if x_k and y_k are the sample input and output signals then we will have:

$$y_n = \sum_{i=0}^{N-1} x_{n-i} C_i = x_n C_0 + x_{n-1} C_1 + \ldots + x_{n-N+1} C_{N-1}$$

Filter coefficients are saved in the program space and the input signal samples are saved in the data space.

Data and program spaces of the DSP are:

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LARP AR0, InputBuf
ADRK N-1
RPTK N-1
MACD Coef, *-
APAC
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This work has been funded by KIATEL Company, IRAN, and has been carried out at the Laboratory of Communication Engineering in Sharif University technology and Develop and Engineering department in KIATEL Company, IRAN. We appreciate Mr. H. Keshvari Asl, the CEO of KIATEL Co.

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[1] Million Instructions per Second

Now the output of the filter is saved in the accumulator. The program algorithm is shown in figure (3).

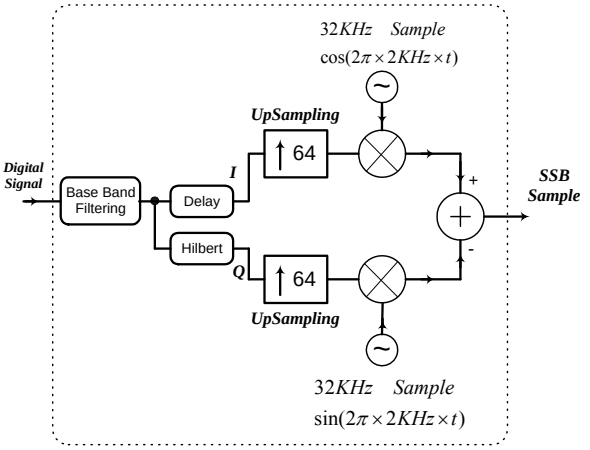
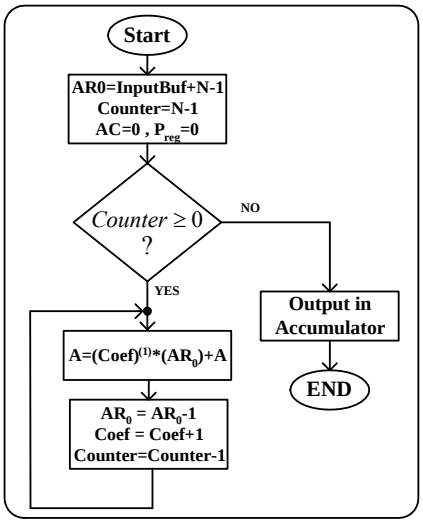


Fig. 2. Block Diagram of the SSB modulator in the DSP processor

The MACD instruction initially adds the P_{reg} and the accumulator and then saves the result of this addition in the accumulator. It will then multiplies the filter coefficient in the input signal and puts this result in the P_{reg}.

The input signal pointer is then decrease by one and the filter coefficient pointer is increase by one, and counter in the MACD loop is also decrease by one and the address where the input signal sample is saved (after multiplying the input signal and the filter coefficient) is increase by one.

MACD Coef, *_
A=Preg +A
Preg = (Coef)×(AR0)
Coef=Coef+1
(AR0+1) = (AR0)
AR0 = AR0-1



(1): (Coef) = Content of Address in Program Memory

Fig. 3. The program algorithm with DSP

When the MACD instruction is put in a repeating loop, it is calculated in the DSP clock cycle and an N-TAP filter is calculated for N cycles (without the Over Head).

Hilbert Converter

One way to build a SSB signal is using a Hilbert converter. By using a FIR filter, we can build a Hilbert filter. Noting that the message signal in the PLC system consists of Voice signal in 300-2000Hz bands and the telegraphy signal in 2000-3400Hz bands, making the above frequency in these bands is easily achieved. Note that the Hilbert filter associated with the voice signal has more taps than that of the telegraphy signal. This is because the voice band filter has to make 180º phase changes in a smaller frequency domain and therefore needs a filter with more taps.

Because voice phase starts from 200Hz, therefore there is no need for 180º phase changes in the 0 frequency spot and we can assume that, with a smaller Tap as shown in figure (4). This is also correct for the telegraphy Hilbert filter and we can design that with fewer taps than the voice Hilbert filter.

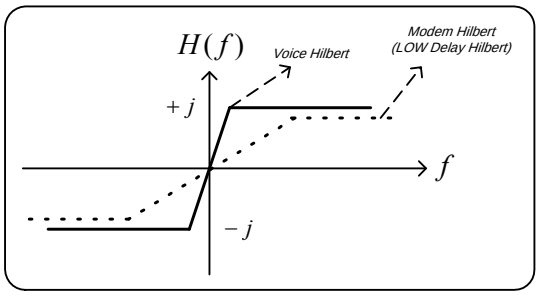


Fig. 4. Frequency response of Hilbert real voice/telegraphy

Noting the acquired information, now it is time to analyze USSB (Upper Single Side Band) and LSSB (Lower Single Side Band) signal in the data transmission system. Assume that the data signal spectrum is as shown in figure (5) (Combination of voice and telegraphy signals)

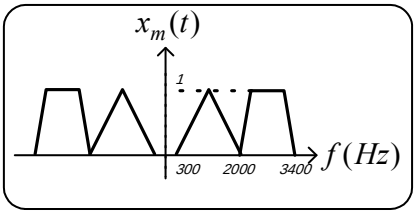


Fig. 5. Data signal spectrum

After passing the message signal through the Hilbert signal, $\hat{x}_m(t)$ signal as shown in figure (6) is created. The $\hat{x}_m(t)$, $x_m(t)$ are then multiplied in sample sinusoidal and cosine carriers and I_{HF}, Q_{HF} signals are created as shown in figure (7).

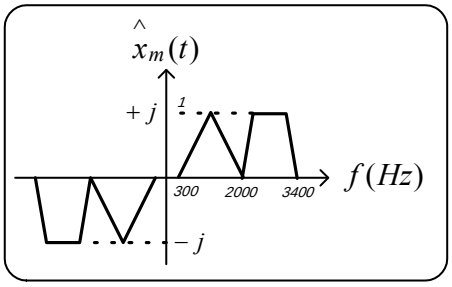


Fig. 6. Data signal spectrum after filtering

Now adding and subtracting these signals easily create the USSB and LSSB signals.

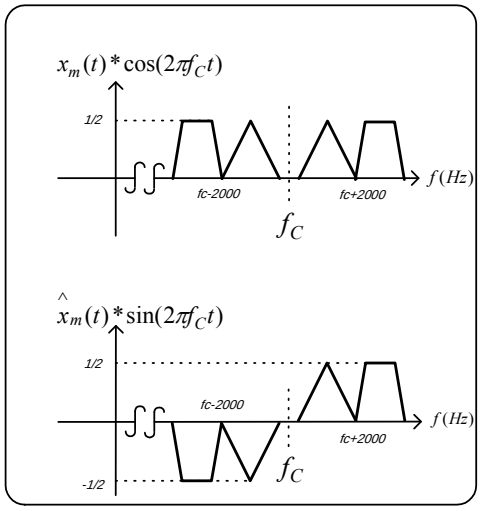


Fig. 7. I & Q signals spectrum after multiplied in sinusoidal and cosine

This card consists of two main parts: Base Band DSP and Supervisory. Each section is described in the following sections:

A. How to create the Sinusoidal signal using DSP

Using the Lookup Table

To create the sinusoidal signal, its samples can be saved in a table and these samples can be read by a sampling frequency.

To have a Sinusoidal with f_d frequency the samples of the table is calculated as follow:

$$x_n = A_C \sin(2\pi f_d t)\Big|_{t=nT_S=n/f_s} = A_C \sin\left(2\pi f_d \, {}^{n}\!/_{f_S}\right)$$

$$2\pi f_d \, {}^{n}\!/_{f_S} = M \times 2\pi \Rightarrow N = M \frac{f_S}{f_d} \Rightarrow \frac{N}{M} = \frac{f_S}{f_d}$$

Therefore, the number of memory cells is achieved from above. It is evident that in some instances, there is need for large memories even though there is no processing being done.

a) Direct calculation of the Sinusoidal signal

The sample Sinusoidal is achieved as follows:

$$x_n = A_C \sin\left(2\pi f_d \frac{n}{f_S}\right) = A_C \sin\theta_n,\ \theta_n = 2\pi f_d \frac{(n-1)}{f_S}$$

and $\theta_n = 2\pi f_d \frac{n}{f_S},\ \Delta\theta = \theta_n - \theta_{n-1} \Rightarrow \Delta\theta = \frac{2\pi f_d}{f_S}$

In these formulas, the $\Delta\theta$ is the chosen sinusoidal frequency. By the above formulas for the sinusoidal and cosine we will have:

$$\sin\theta_n = \sin(\theta_{n-1} + \Delta\theta) = \sin\theta_{n-1}\cos\Delta\theta + \cos\theta_{n-1}\sin\Delta\theta$$

$$\cos\theta_n = \cos(\theta_{n-1} + \Delta\theta) = \cos\theta_{n-1}\cos\Delta\theta - \sin\theta_{n-1}\sin\Delta\theta$$

It will be enough to actuate these return functions by an initial θ0 (where this initial value is arbitrary). It is apparent that by each calculation of the above return functions, the sinusoidal and cosine is calculated. In this method there is no need for large memories. However, there is need for 4 multiplying and two addition processes.

A very important point in the above functions is that because of calculation errors and digitization, these functions might diverge and a distorted sinusoidal signal is then created. To solve this problem after each multiplying the necessary rounding needs to be done and these errors needs to be corrected. This by itself creates more calculations.

b) Reaching a middle ground

In this method, the [0,2π] domain is divided into N equal sections, (N is chosen according to the resolution power needed). Now the sinusoidal is calculated in all the N sections and is saved in a table.

$$\theta = \theta_C + \delta\theta$$

Where θc is the quantized θ (where the trigonometric values of them have been saved in the table). The $\delta\theta$ is the difference between the θ and the θc value. Therefore:

$$\sin(\theta) = \sin(\theta_C + \delta\theta) = \sin\theta_C \cos\delta\theta + \cos\theta_C \sin\delta\theta$$

$\sin\delta\theta$ And $\cos\delta\theta$ are calculated using following approximations:

$$\sin\delta\theta \cong \delta\theta \quad or \quad \sin\delta\theta \cong \delta\theta - \frac{\delta\theta^3}{3!} \text{ and } \cos\delta\theta \cong 1 - \frac{\delta\theta^2}{2!}$$

c) Using IIR filter to create a sinusoidal signal

One affective and useful way to create sinusoidal signal is using IIR filters. In this method by a multiplying process and two memories the sinusoidal wave can be created as follows:

$$y_n = \sin\theta_n, y_{n+1} = \sin\theta_{n+1} = \sin(\theta_n + \Delta\theta),$$

$$y_{n-1} = \sin\theta_{n-1} = \sin(\theta_n - \Delta\theta)$$

Therefore:

$$\Rightarrow y_{n+1} = 2\cos\Delta\theta y_n - y_{n-1} \text{ and } \Delta\theta = \frac{2\pi f_d}{f_S}$$

Here $\Delta\theta$ is the output frequency.

B. Creating a SSB demodulator using DSP

The modulated SSB signal is passed through a band pass filter which is almost selective (The filter response can be seen in figure (8)) and is then entered an A/D. Noting that the working PLC frequency band is 40-400kHz, by abiding to the Nyquist sampling rate, the clock frequency pulse is chosen 2.048MHz. The received digitized signal is multiplied in the sinusoidal and cosine signals equal to $f_R - 2KHz$ and I - Q components are created. 64 then down sample these samples.

The Q component is passed through a Hilbert filter in the 2-6 kHz band and are added with the delayed I components, (Until the delay created in the Hilbert filter is compensated).

Eventually, the real message signal is created in a modulated format and the frequency of 2 kHz. By absorbing the 2 kHz sinusoidal and cosine samples, (that where created from the PLL), the base band message signal is displayed.

The Hilbert filter is shown in figure 9 and can deduct a display channel that resides 8 kHz from the main channel.

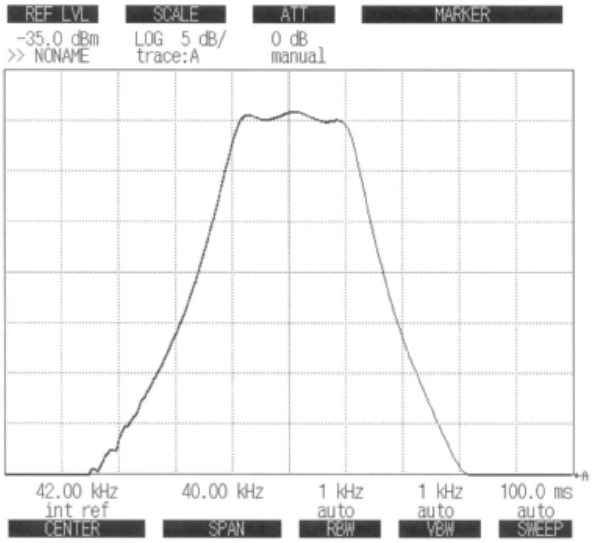


Fig. 8. Selective band pass filter response

The SSB demodulator block diagram in the Fixed-Point DSP processor is shown in figures (9 and 10).

IV. Conclusions

The PLC systems existing in the electrical network are mainly analog and old and are high cost. Also these systems come in large sizes. Using digitized systems we can create great flexibility in design of the system and also deduce the size and the price. Also system abilities are expanded in this method. In signal processes, parameters such as memory, process speed, and sampling frequency are very important. To create different sections of the SSB modem, optimizing methods and procedures have been the goal. The procedures chosen for filtering is for optimizing time. This is because the speed in the signal processing is very important. This is especially true in the HF section where the signal frequency is also high and there is little time between one signal sample and the next.

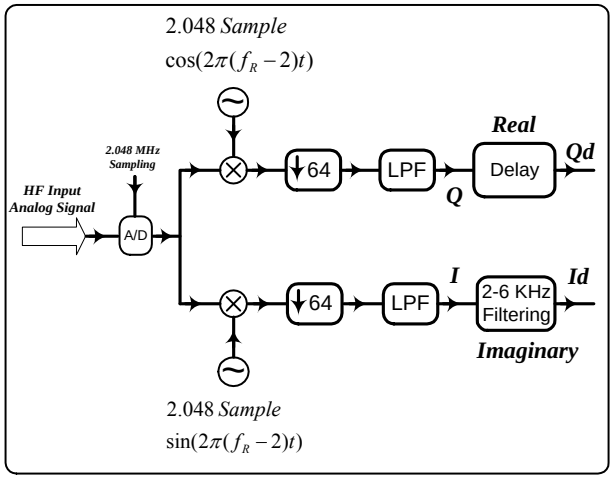


Fig. 9. SSB modulator block diagram in Fixed-Point DSP processor

According to identical algorithms the DSP TMS320C5402 is two times faster than the DSP TMS320C50.

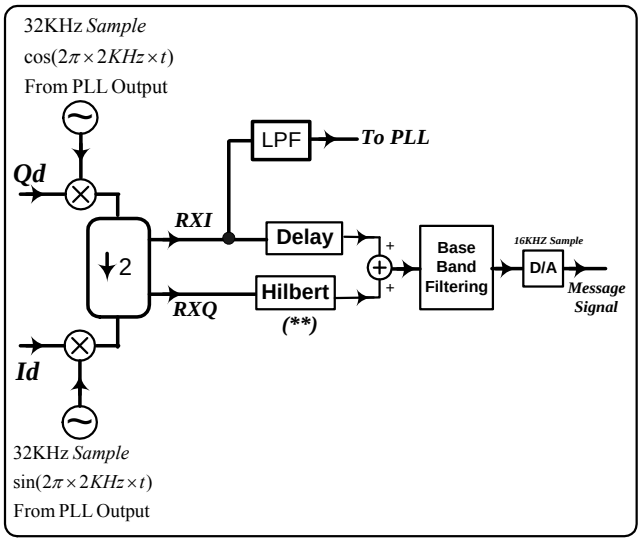


Fig. 10. SSB modulator block diagram in Fixed-Point DSP processor

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