Dual Dynamic Biasing with Input Power Pre-compensation for Class-A/AB enhancement

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***Abstract* — A novel dynamic biasing methodology specially oriented towards high-efficiency class-A/AB design is presented. To achieve flexibility in the efficiency/linearity tradeoff, the gate and drain voltages as well as the input power are varied as a function of the desired output power. The aim is Power Added Efficiency (PAE) maximization restrained by linearity conditions. Simulation results for a 30dBm GaAs pHEMT amplifier yielded gain levels between 10.5 and 11dB for the whole power range, phase variation limited to 2.6° only. The PAE was found to be 25% in average over the dynamic range. This is three times as large as the static bias case. The second and third harmonic vary from -58dBc to -25dBc and -62dBc to -42dBc respectively hence preserving linear behavior.**

***Keywords* — Dynamic bias, envelope tracking (ET), smart biasing, high efficiency, class-A amplifiers, slice plots, contours.**

I. Introduction

MODERN modulation formats have highly varying envelope signals in order to optimize the use of spectral resources. To avoid nonlinear distortion a high-linearity class-A amplifier is typically used at several dB of back-off, which has the side effect of dramatically decreasing efficiency [1].

The approach of smart bias variation in non-switching amplifiers goes back to Envelope Tracking (ET), where the principle was to continuously adjust the drain bias voltage of a class-B amplifier according to the envelope power of the input signal [1]. For the case of a class-A amplifier K. Yang et al. [2] showed that Power Added Efficiency (PAE) is nearly three times as much when gate and drain feeds are varied together continuously compared to the case when they are varied separately; and that PAE increases by a factor of 8 compared to a static bias case (i.e., constant supply voltages).

A different approach to the bias variation problem was proposed in [3]. Pairs of input power and drain bias values (P_{in},V_{DD}) are chosen so that for a given fundamental output power level (P_{out}) the DC power consumption is minimized. The same principle is used in [4] for Switching Mode amplifiers but considering also the output phase dependency on the input phase, input power and drain bias. By evaluating a path for maximum PAE and a path for constant phase for each P_{out} level, it was shown that the bandwidth of the DC/DC converter and of the input to the amplifier was smaller for the constant phase path while PAE was still high.

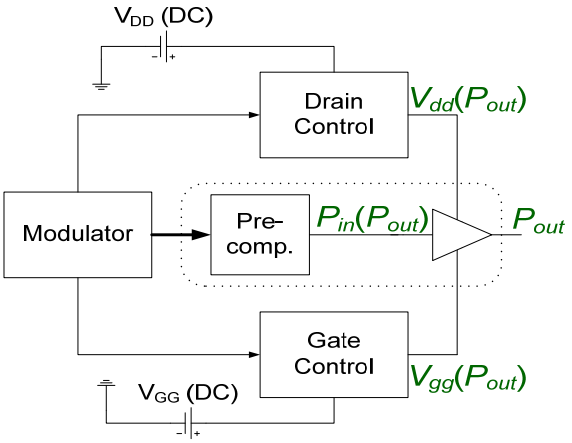

Figure 1. Simplified block diagram of the Dynamic Biasing system for class-A/AB amplifier enhancement.

This work endeavors to establish a new design methodology for dynamically biased class-A/AB amplifiers; which studies the synchronized variation of gate and drain voltages together with the input power thus establishing a "dynamic bias path". These three degrees of freedom will allow us to explore not only maximum PAE or constant output-phase variation paths [3, 4] but also many others that will be chosen according to specific design goals at the output (i.e., maximum output power, gain level and flatness and second and third harmonic power).

Figure 1 shows a simplified diagram of the DB system. Note that the output power of the amplifier is set by the modulator which in a digital or analog fashion acts over the gate and drain controls, as well as the pre-compensation stage. Digital Pre-distortion (DPD) can be included in the pre-compensation stage (PCS) if desired. Mathematically, the goal is to run a 1-tone static characterization on the PA to determine 3 functions: $V_{GG}(P_{out})$, $V_{DD}(P_{out})$, $P_{in}(P_{out})$ along the whole output power range.

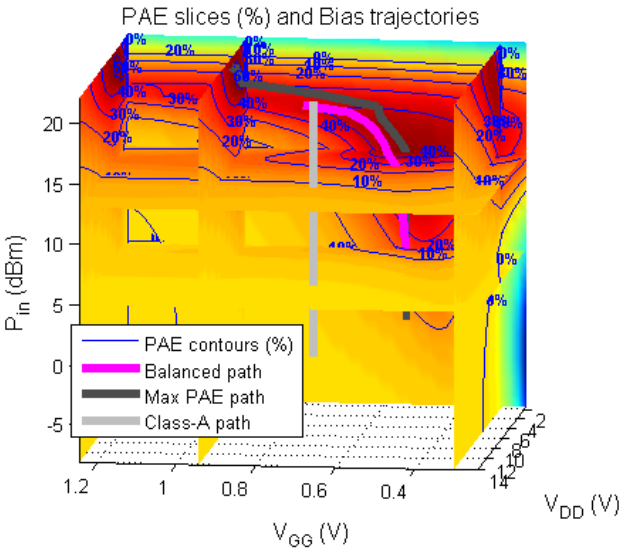

Figure 2. PAE and Pout slices and contours with bias trajectories for balanced linearity/efficiency, maximum PAE and class-A operation.

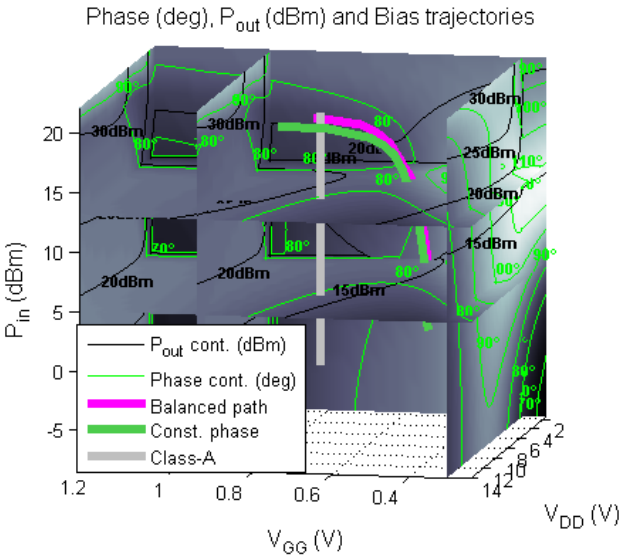

Figure 4. Phase and Pout slices and contours with bias trayectories for balanced linearity/efficiency, constant phase and class-A operation.

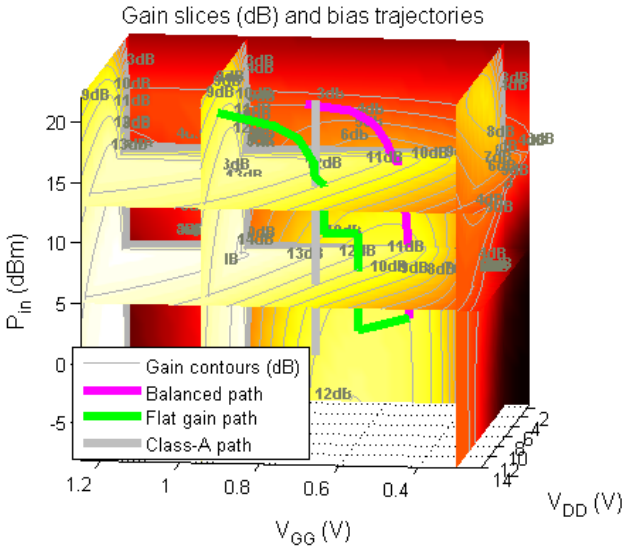

Figure 3. Gain slices and contours with trajectories for balanced linearity/efficiency, flat gain and class-A operation.

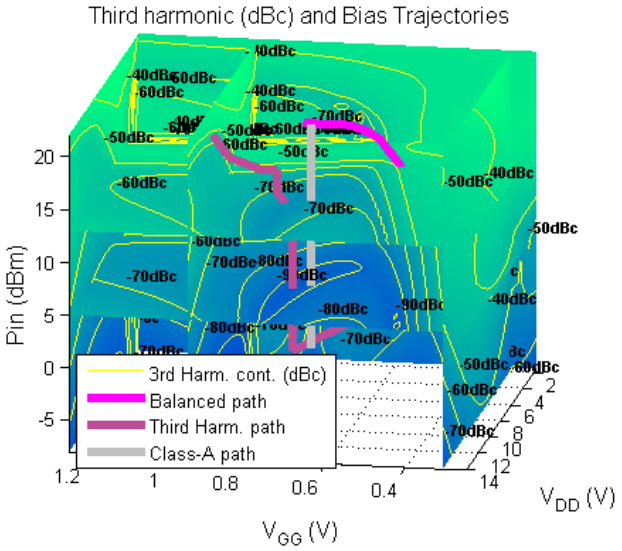

Figure 5. Third harmonic slices and contours with bias trayectories for balanced linearity/efficiency, minimum 3rd harmonic and class-A operation.

The outline of this paper is as follows: Section II presents the 30dBm pHEMT class-A amplifier used in the DB system and describes the settings for the simulation. Section III presents a 4D slice-contour graphical method to view several of the output parameters (e.g., P_{out}, PAE, etc.) as a response to different bias points and input power; and also analyzes different paths and their position within the contours. Section IV shows the resulting output properties for each of the paths and Section V summarizes draws some relevant conclusions.

II. Power Amplifier and Setup

A 30dBm GaAs amplifier was designed using Advanced Design Simulation software together with Triquint's Toolbox. The amplifier has two lumped-component high-pass and low-pass matching networks at input and output respectively. The output matching was optimized for maximum gain.

A one-tone simulation was run on the amplifier sweeping the input power levels from -8dBm to 22dBm in uniform 1dB intervals while also varying V_{GG} and V_{DD} from 0.25V to 1.25V, 1.5V to 14Vin steps of 0.02V and 0.25V respectively. The required currents and voltages for each (V_{GG}, V_{DD}, P_{in}) combination are imported into MATLAB in order to calculate the output power, PAE, gain, phase shift with respect to the input phase, 2nd and 3rd harmonic distortion. This "one-tone design" approach is justified by assuming that the amplifier is memoryless within the operation bandwidth, and no thermal effects are accounted for either.

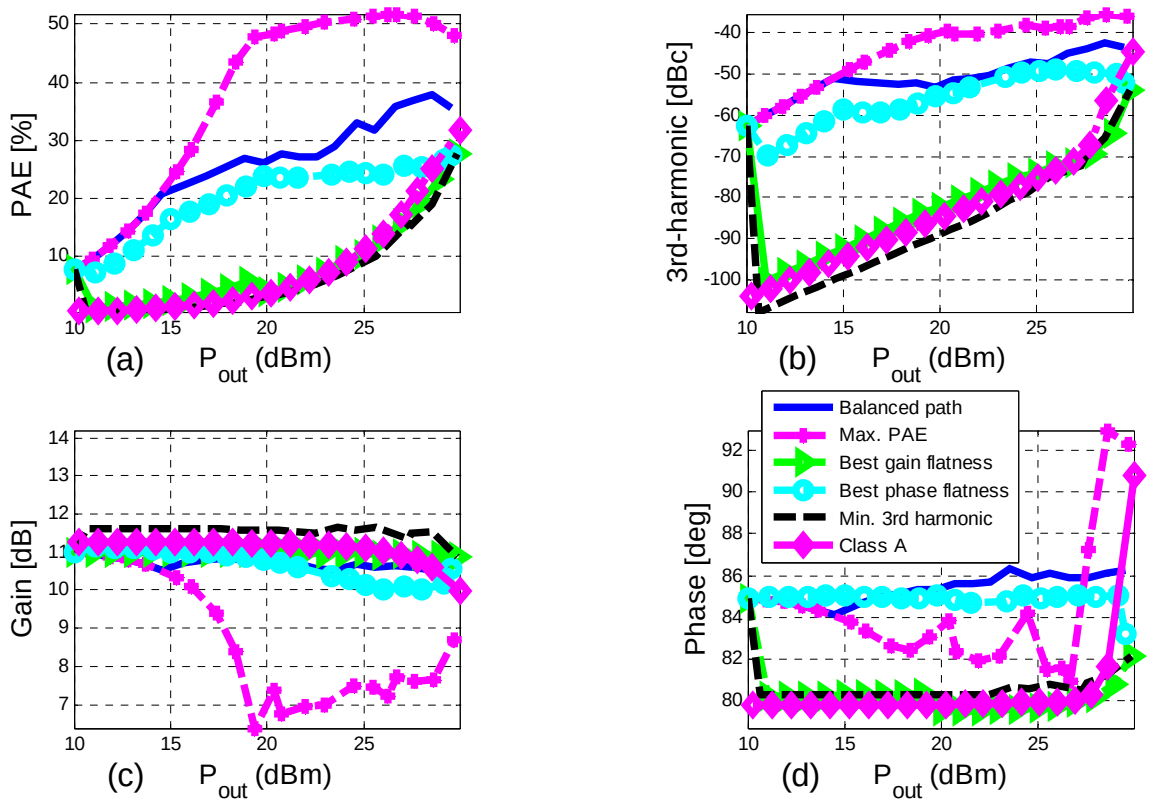

Figure 6. Results for the DB paths. (a) PAE (b) 3rd harmonic (c) Gain (d) Output phase

III. Slices and Contours as a 4D Graphic Method for Different Biasing Paths

In order to extract design information from such a large amount of data it becomes indispensable to evaluate the magnitude and variation of the output quantities within the different regions of operation in the (V_{GG}, V_{DD}, P_{in}) space in order to find a path that fulfills the linearity/efficiency requirements. A new visual representation method[1] was devised where a 4D slice-contour plot is used for the (V_{GG}, V_{DD}, P_{in}) axis. The magnitude of the output quantities is represented in colors and labeled by contours, thus becoming the 4th dimension, as shown in figures 2-5. In general, low drain voltages correspond to the switching region of the amplifier. One can identify linear zones over the Pin slices (paralell to the VDD-Pin plane) by seing that the Gain contours in Figure 3 should tend to have smooth variations over the V_{DD} axis and should tend to be constant over the Pin slice. Low V_{GG} and moderate V_{DD} (i.e., below 7V, in this case) correspond to the deep class-AB or B biasing regions, were higher PAE and higher harmonics are expected compared to class-A biasing. Six different paths are illustrated in the figures: max. PAE, max. gain, min. phase shift, min. third harmonic distortion and finally a balanced path that attempts to combine linearity and efficiency.

The maximum PAE path in Figure 2 tends to keep the drain voltage feed low near to the swithing region. This yields high efficiency but high harmonic distortion. The balanced path starts with low VGG and VDD but as the output power increases it tends to stay at a distance from the high-efficiency nonlinear area. The class-A path, starts at a lighter zone and stays there all along reaching only the 10% PAE contour

From Figure 3 and Figure 4 it becomes clear that the gain is very low for low V_{GG} and/or V_{DD} values and that the phase varies abruptly between 70 and 100 deg. The third harmonic in Figure 5 starts from a low -90dBc region, which is near to the class-A path, and follows a straight line perpendicular to the VGG-VDD plane, similar to the class-A case, for most of the Pout values, until it bends increasing V_{GG} strongly towards the end.

Based on this figures and on the application requirements one could find a suitable starting point for the dynamic bias path and determine the optimum zone that such a path must traverse. A special algorithm fully described in [5] was specially designed for the purpose.

IV. Output Properties of the DB Paths

Figure 6 presents the results at the output of the PA for each path. The max. PAE path has the highest efficiency of all but has also a very high third harmonic, rapidly varying phase and a gain drop from 11 to 6dB, which makes it useless for practical purposes. Even if the gain was linearized, the power loss could only be compensated for

[1] The slice plots are new in the sense that there is no literature reporting their use in the Power Amplifier field to the knowledge of the authors.

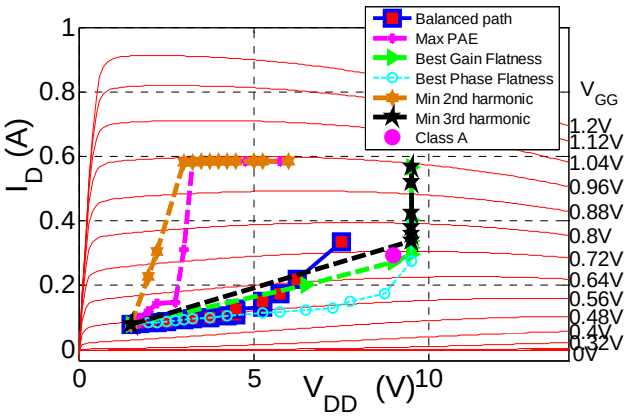

Figure 7. Location of the DB paths in the IV plane.

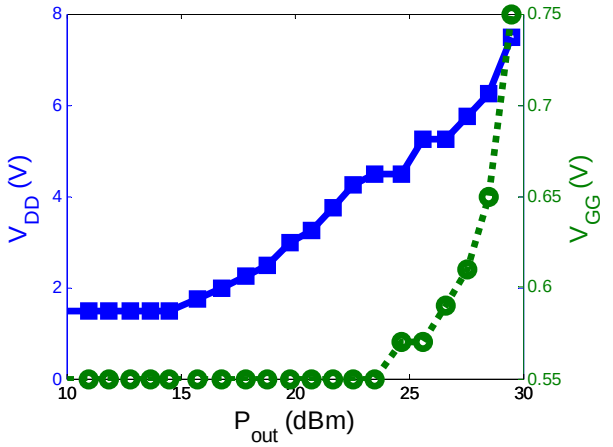

Figure 8. Bias as a function of output power for the balanced path.

by a boosting amplifier.

The "balanced path" still provides a significant PAE improvement with respect to the class-A PA and has lower third harmonic compared to the maximum PAE path. It was engineered for low gain and phase variations, which is shown in Figure 6 where the gain is steady between 10.5 and 11dB and the phase varies between 84 and 86 deg only. Note that the "best phase flatness" path has similar characteristics. Alternatively, the "best gain flatness" path is very close to the class-A PA up to 27dBm though it follows a very different trajectory (see Figure 3). At 27dBm of P_{out}, however, the class-A tends to have a big phase-jump as it reaches compression while the best gain flatness path holds the gain and phase constant while the 3rd harmonic is lower than for the class-A PA. In this case the DB acts more as a linearization mechanism than as an efficiency enhancement method. The trajectories of the paths in the IV plane are shown in Figure 7. Each marker accounts for a 1dB increase of Pout, hence giving a sense of how fast the bias changes with output power. Note that while several paths tend to have an abrupt current increase for the last P_{out} values, the balanced path continues to show a moderate increase both in drain current and drain voltage.

Finally, from Figure 8 it can be seen that $V_{GG}(P_{out})$ and $V_{DD}(P_{out})$ could be conveniently approximated by a simple low-order polynomial for the balanced path.

V. Conclusion

After describing a Dual-Dynamic Bias system and studying different combinations of bias and input power for the different output power levels, it becomes clear that the effect of dual dynamic biasing on the output properties of the amplifying system can change depending on the region of the (V_{GG}, V_{DD}, P_{in}) space that is chosen; and that the purpose of the Dynamic Biasing can vary between two extremes: pure efficiency enhancement and linearization method. A relevant consideration for future work is the bandwidth requirement for the DC/DC converters and the pre-compensation system on the implementation of the $V_{GG}(P_{out})$, $V_{DD}(P_{out})$ and $P_{in}(P_{out})$ functions. This becomes especially important at the drain since it is difficult to vary high currents rapidly in an efficient manner.

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