A Cost-Based Path-Search Algorithm for Enhanced Design With Dynamic Bias

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***Abstract* — A novel algorithm for class-A/AB power amplifiers (PA) enhancement is fully described. The principle is to find a combination of base current (gate voltage), collector voltage (drain voltage) and input power for each output power level so that the linearity/efficiency specifications of the application are satisfied. Based on a 1-tone static characterization of the amplifier, the algorithm uses a cost function that maximizes Power Added Efficiency (PAE) while minimizing gain variation, phase shift, and second and third harmonic power levels. The algorithm was applied to a pHEMT amplifier and a HBT transistor. Single-tone measurements on the HBT transistor show an average PAE of 28% along the output power range, compared to the simulated 8% of a normal class-A.**

***Keywords* — Bias trajectory, dynamic bias, efficiency, HBT, linearity, pHEMT, power amplifier**

I. Introduction

It is well known that the RF power amplifier (PA) is a key device in the telecommunication's system hardware. It must boost the power of the RF signal before the transmitting antenna and have low distortion [1]. As means to maximize spectral efficiency, sophisticated modulation formats such as OFDM and high order QAM modulations are deployed together with pulse-shaping filters, which in turn increases the Peak to Average Power Ratio (PAPR) of the RF signal [2]. Class-A/AB amplifiers are typically utilized with several dB back-off to reduce non-linear distortion. This will severely diminish the efficiency of the PA and of the whole transmission chain [3].

Though polar transmitter architectures with high efficiency switching mode amplifiers would be a good solution for efficiency/linearity trade-offs, class-A/AB amplifiers are still heavily used and thus Envelope Tracking alternatives represent a practical advantage [4]. It was shown in [5] that varying the gate and drain continuously could increase the Power Added Efficiency (PAE) of a class-A PA by a factor of three respect to the single bias variation case. Cesari in [6] presented the idea of varying the input power together with the bias according to the desired output power level, while the same principle was applied to switching-mode amplifiers in [7] accounting for the output phase as controlled by the bias/input power variation. The authors have already explained in [8] that many other output variables could be taken into account in order to make design more flexible; such as gain level, gain flatness, PAE, phase shift, second and third harmonic distortion. A graphic 3D method to visualize the different regions of each of the output parameters in terms of gate bias, drain bias and input power *(Vgg, Vdd, Pin)* was also explained. This paper approaches the task of finding a numeric method to determine a *(Vgg, Vdd, Pin)* combination for each desired output power level (bias trajectory). A HBT transistor is used as a test device therefore the *(Vgg, Vdd, Pin)* points simply become the *(Ib, Vce, Pin)* points. This algorithm uses static one-tone simulation results with swept base current, collector voltage and input power *(Ib, Vce, Pin)* and has many configuration parameters which can be set by using the a priori information of the 3D slices and contour plots [8]. The system evaluates different PA parameters and attempts to combine linearity and efficiency leading to a tuned (balanced) bias trajectory. Memory and thermal effects are disregarded.

II. Tracing a Path

Although the main purpose of dynamic biasing is to increase the efficiency of a class A amplifier, linearity has to be considered as well. Therefore, an acceptable bias trajectory should not allow the transistor to enter the current saturation region nor the Class B region for noticeable *Pin* levels. The path could start for example in the Class B region where efficiency is higher and linearity good for low input power levels. Then, as *Pin* increases, it should move toward the linear Class A region, staying as close as possible to the very efficient switching zone [8]. As close as possible means close enough not to get high harmonic distortion.

Since the algorithm performances depend a lot on the start point selection (point having the lowest *Pout*), its constraints should be set properly. In fact the algorithm seeks for high-efficiency, low-harmonic distortion points and tries to keep output phase and gain as flat as possible. Therefore, in order to guarantee acceptable linearity, they

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should be close to the gain and output phase the amplifier exhibits in its linear region. Hence, a linear and efficient area has to be identified and then the searching script will automatically choose the point having the highest PAE within it. For instance, that could be the Class B region for low input powers [8].

A. Searching Algorithm

The developed algorithm should be first correctly set up and then run. During the explanation the algorithm is considered as applied to a HBT amplifier.

B. Constraints

The constraints the user should define before running the algorithm are listed below:

- **Output power range**, the algorithm will try to find a bias path for the user defined output power range
- **Global *Ib* and *Vce* constraints**, points having lower or higher *Ib* and *Vce* are discarded.
- **Start point constraints,** constraints the user can act on to make the algorithm find a suitable starting point.
- ***Ω* cost function weights**, weights of the coefficients that combine into the cost function (7).
- **(*Ib*, *Vce*, *Pin*) space distance normalization coefficients**, the algorithm uses a normalized (*Ib*,*Vce*,*Pin*) distance.
- **Class A bias point**, a normal class A bias point has to be chosen to compare the performances of a dynamically biased amplifier to those of a classic one.

C. Sorting 3D Points

At the beginning, the script sorts the *(Ib, Vce, Pin)* points according to their output power levels, forming the so called *Pout* groups. For the HBT, power levels from 0dBm to 20dBm with a step of 1dB, have been considered. The first group contains points that give between −0.5dBm and 0.5dBm of power, the second one contains those that give between 0.5dBm and 1.5dBm of power and so on. The program will later select one point per each group and thus find a suitable bias path.

D. Start Point

Afterwards, the program seeks for a start point within the first output power group. The sequence listed below is followed and the start point constraints are applied.

1. A square in the *Ib*, *Vce* plane [8] is defined and forces the algorithm to choose a start point within its limits.
2. Points with transducer gain lower than a certain value are discarded. This limit should be close to the minimum gain the amplifier exhibits in its linear region.
3. Points with output phase out of a user defined range are discarded. This range should not differ too much from the phase the amplifier's output has in its linear region.
4. Points having second harmonic power level and third harmonic power level higher than certain limits are discarded.
5. Finally, among the points left, the one having the highest power added efficiency is chosen.

E. Following Points of the Path

Once the first point has been set, the following ones are selected. The software proceeds sequentially, considering one output power group at a time in ascending order.

Given the current step *n*, the algorithm considers the point selected the step before *(n − 1)* and excludes, among the current group *n*, all the points having lower bias signals (*Ib* and *Vce*) as well as lower available powers from the source (*Pin*). This makes *Ib* and *Vce* not too complicated functions of *Pout* and guarantees a monotonic *Pin − Pout* relation.

Now, all of the *M* points left are suitable candidates. Then, *M* different trajectories are evaluated. Each of them has, as its last *nth*-step point, one among the *M* left ones, while all the others (steps *1,...,n−1*) are the points the algorithm has selected before. Therefore, all the *M* trajectories differ only in their *nth*-step point. Six parameters have been introduced to evaluate these paths and choose the most suitable one:

α, average power added efficiency ($PAE_{\%}$), (%)

$$\alpha = -\frac{1}{n}\sum_{i=1}^{n} PAE_{\%,i} \tag{1}$$

β, transducer gain (G_{dB}) flatness index, (dB)

$$\beta = \sum_{i=2}^{n} |G_{dB,i} - G_{dB,i-1}| \tag{2}$$

γ, output phase (Φ_{deg}) flatness index, (deg)

$$\gamma = \sum_{i=2}^{n} |\phi_{deg,i} - \phi_{deg,i-1}| \tag{3}$$

δ, average second harmonic power (SH_{dBc}), (dBc)

$$\delta = \frac{1}{n}\sum_{i=1}^{n} SH_{dBc,i} \tag{4}$$

ε, average third harmonic power (TH_{dBc}), (dBc)

$$\epsilon = \frac{1}{n}\sum_{i=1}^{n} TH_{dBc,i} \tag{5}$$

dist, normalized distance between current point and previous one in the *(Ib, Vce, Pin)* space

$$dist = \sqrt{\left(\frac{Ib_n - Ib_{n-1}}{Ib_{NORM}}\right)^2 + \left(\frac{Vce_n - Vce_{n-1}}{Vce_{NORM}}\right)^2 + \left(\frac{Pin_n - Pin_{n-1}}{Pin_{NORM}}\right)^2} \tag{6}$$

Each evaluated path has its own parameters. Therefore, α, β, γ, δ, ε and *dist* are actually arrays with their indexes identifying a certain path.

The arrays are then normalized to their absolute maxima and, point by point, linearly combined into a cost function called Ω:

$$\Omega = w_\alpha \alpha_{norm} + w_\beta \beta_{norm} + w_\gamma \gamma_{norm} + w_\delta \delta_{norm} + w_\epsilon \epsilon_{norm} + w_{dist}\, dist_{norm} \quad (7)$$

with

$$w_\alpha + w_\beta + w_\gamma + w_\delta + w_\epsilon + w_{dist} = 1 \quad (8)$$

Finally, the path having the lowest Ω parameter is chosen, its point from the current output power group (n) selected for the final path and the algorithm moves on until a complete path is identified. This path is called the tuned trajectory.

Normalization is necessary to give all the parameters the same importance. Then, the weighted sum makes some parameters more relevant and others less relevant, depending on what kind of tuned path the software should seek for.

The minus sign in the α parameter formula (1) simply turns the maximization problem into a minimization one.

The distance parameter *dist* has been introduced not to have abrupt jumps in the final trajectory and therefore obtain a more continuous curve in the *(Ib, Vce, Pin)* space. If one variable has not to vary too much while moving from one trajectory point to the next one, then it should be weighted more, giving a higher distance.

Hence, the searching criteria can be modified through the following parameters yielding different trajectories:

- w_α: Power added efficiency weight
- w_β: Gain flatness weight
- w_γ: Output phase flatness weight
- w_δ: Second harmonic output power weight
- w_ϵ: Third harmonic output power weight
- w_d: Distance weight
- Ib_{NORM}: *Ib* normalization coefficient
- Vce_{NORM}: *Vce* normalization coefficient
- Pin_{NORM}: *Pin* normalization coefficient

There is no rule on how to set all the coefficients described before. As a rule of thumb, one could start with the coefficients listed in Table 1.

TABLE 1: SUGGESTED INITIAL COEFFICIENTS

Coefficient	Suggested initial value
$w_\alpha, w_\beta, w_\gamma, w_\delta, w_\epsilon, w_{dist}$	1/6
Ib_{NORM}	*max Ib from HB sweep*
Vce_{NORM}	*max Vce from HB sweep*
Pin_{NORM}	*max Pin from HB sweep*

III. RESULTS

An integrated InGaP emitter HBT transistor from TriQuint Semiconductor has been chosen as a test device for the analysis described in [8] and the algorithm presented before.

The selected working frequency is 1.9GHz and output power levels from 0dBm to 20dBm are considered.

Results show a tuned trajectory with an average PAE of 27.5%, while the simulated class A average PAE is 8% (Fig. 3). Gain and output phase variations are limited: 1.5dB of maximum variation for gain and 2° for phase (Fig. 4 and Fig. 1). Yet, *Ib* and *Vce* do not have complicated control functions (Fig. 2). Harmonic distortion is relevant, in particular the second harmonic reaches −17dBc and the third one −25dBc [9].

According to the two tones ADS simulation, at high *Pout*, the third order IMP grow up to −27dBc (Fig. 5) and the fifth order IMP to −31dBc [9].

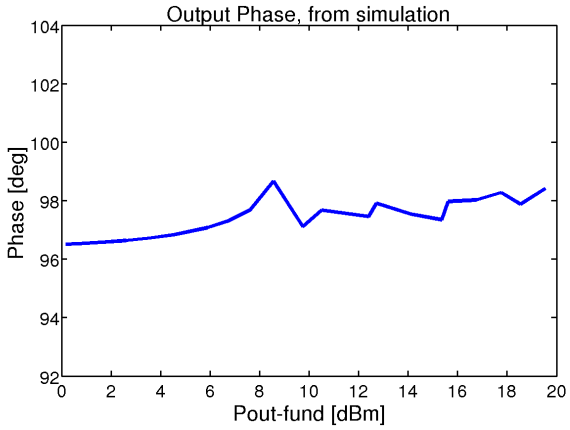

Fig. 1, Tuned trajectory output phase as function of Pout (simulated)

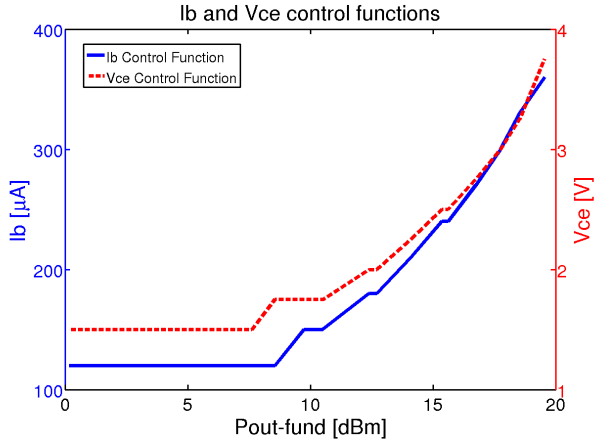

Fig. 2, Tuned trajectory *Ib* and *Vce* control functions: *Ib* continuous blue line with axis on the left side, *Vce* dashed red line with axis on the right side

IV. MEASUREMENTS

The device has been tested in the laboratory. For each of the trajectory bias points the following static measurements have been executed: DC measurements, one tone

measurements and two tones measurements. Power added efficiency, gain, harmonic distortion and intermodulation products are all experimentally estimated. Phase measurements could not be performed.

Measurements show good agreement with simulations. There are no big discrepancies and only the harmonics are higher than expected. The second harmonic reaches −14.5dBc while the third one −21dBc [9]. Nevertheless, the ADS transistor model describes the device very well. The measured average PAE of the tuned trajectory is 28.2% (Fig. 3), which is even higher than what expected (27.5%). The measured gain is a bit higher at the beginning but its maximum variation is, as expected, limited within 1.4dB (Fig. 4).

Two tone measurements show that intermodulation products behave mostly as predicted (Fig. 5 and [9]). The third order IMP do not exceed −25dBc and the fifth order IMP reach −30dBc. These values may be acceptable since the dynamic range of the modulated signal is defined by its probability distribution function [2], hence the PA will not always deliver the highest *Pout* and IMP products should be lower. Yet, a DPD system could decrease the adjacent channel power ratio (ACPR) even more. Compared to one tone measurements, when two tones are present at the input the average PAE drops to 27.1% and the measured gain is at most 0.4dB lower (see [9]).

Finally, measured results may differ from simulations due to self-heating.

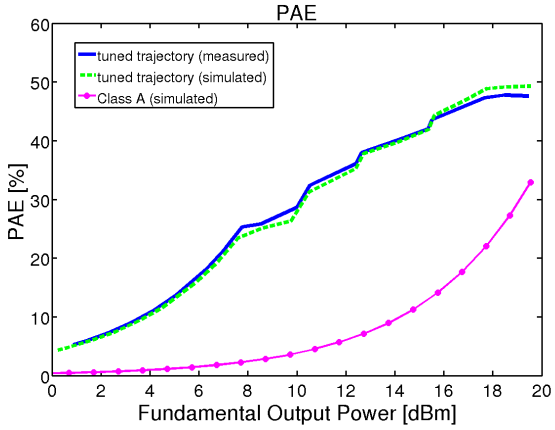

Fig. 3, Tuned trajectory PAE (measured and simulated) compared to Class A PAE (simulated)

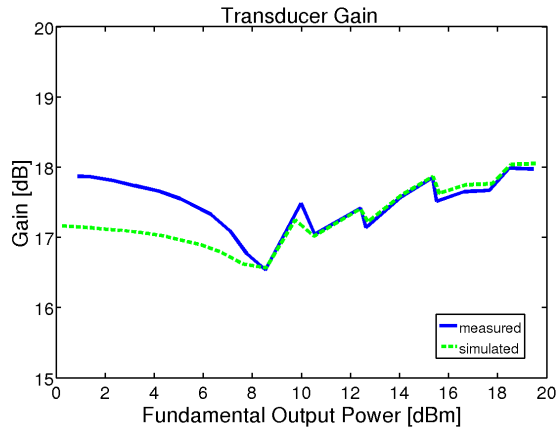

Fig. 4, Tuned path transducer gain, measured (continuous line) and simulated (dashed line)

V. Conclusion

Results show that the developed tool can increase the efficiency of class A PAs and limit their non linearities. Furthermore, an efficient bias path for a pHEMT amplifier has been found ([8] and [9]) and the analysis performed in both the cases (HBT and pHEMT) are conceptually identical. Therefore, a general dynamic bias method could be defined since the presented concepts, analysis methods and implementation algorithms are consistent.

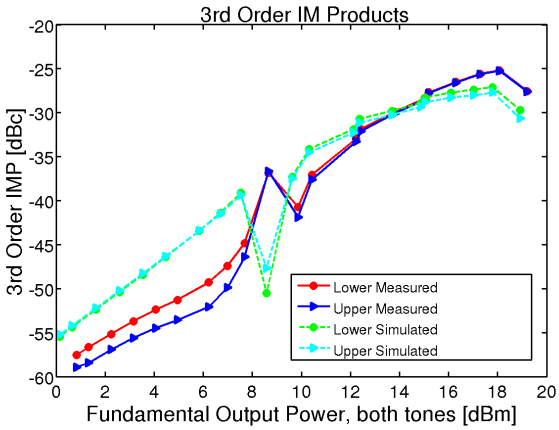

Fig. 5, Third order intermodulation products along the tuned trajectory: measured (continuous curves) and simulated (dashed curves)

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